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Research Article

EXPERIMENTAL INVESTIGATIONS OF RPWM WITH SPWM STRATEGIES OF A SINGLE PHASE CASCADED MULTILEVEL INVERTER

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ABSTRACT
Modern day power systems, power electronic devices are playing vital role in every aspect of the power system network. Among various devices multi-level inverters are the most efficient devices due to their simple circuit configuration, reliability and cost effective implementation. Different techniques are carried out using multi level inverter and its performance was studied. The techniques used are PD, POD and APOD. Comparative study is made between these techniques. Application of Multilevel Inverter using RPWM (Random Pulse Width Modulation) technique improves the operation and utilization of power system and also reduces electromagnetic interference and it as less acoustic noise as compared to other techniques. Simulation result is illustrated for single phase cascaded for PD, POD and APOD techniques, and compared with the RPWM simulation result for different modulation index varying from 0.6 to 1.
The proposed RPWM strategies for cascaded Five Level Multilevel Inverter are effective compared with the Triangular carrier strategy in terms of THD (Total Harmonics Distortion).

Keywords: *RPWM, Triangular Carrier, CMLI, FPGA, THD*

INTRODUCTION
Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. The concept of multilevel converters has been introduced since 1975. Nabae *et al.,* (1981) suggested a new neutral-point-clamped Pulse Width Modulation (PWM) inverter composed of main switching devices which operate as switches for PWM and auxiliary switching devices to clamp the output terminal potential to the neutral point potential has been developed. This inverter output contains less harmonic content as compared with that of a conventional type. Two inverters are compared analytically and experimentally. In addition, a new PWM technique suitable for an ac drive system is applied to this inverter. The neutral-point-clamped PWM inverter adopting the new PWM technique shows anexcellent drive system efficiency, including motor efficiency, and is appropriate for a wide-range variable-speed drive system. Takahashi and Mochikawa (1985) introduced a simplified method to calculate harmonic currents of an induction motor and optimum PWM switching patterns to minimize the harmonic loss are presented. Neglecting the harmonic iron loss, the harmonic loss of the motor is proportional to the square of the RMS current. The waveform of the harmonic current is approximately equal to that of the leakage reactance applied to the same PWM voltage. Its approximation error is very small under normal operating condition. The main results obtained using these approximation are as follows: 1) the optimum PWM patterns of the pulse number from seven to 41; 2) how to choose the

optimum pattern and calculate it by using a computer; 3) the effect of a resistance of the windings and skin effect of the secondary conductor; and 4) microcomputer PWM optimum voltage control schemes. Comparison with other controls is shown by using experimental and calculating results and confirms the effectiveness of this control scheme. Carrara *et al.,* (1992) gave idea about generalization of the pulse width modulation (PWM) sub harmonic method to control single-phase or three-phase multilevel voltage source inverters (VSI) is considered. An analytical expression of the spectral components of the output waveforms covering all the operating conditions is derived. The analysis is based on an extension of Bennet's method. The improvements in harmonic spectrum are pointed out, and several examples are presented, which prove the validity of the multilevel modulation. Peng and Lai (1996) discussed Multilevel voltage source converters which emerging as a new breed of power converter options for high-power applications. The multilevel voltage source converters typically synthesize the staircase voltage wave from several levels of DC capacitor voltages. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The techniques to balance the voltage between different levels normally involve voltage clamping or capacitor charge control. There are several ways of implementing voltage balance in multilevel converters. Without considering the traditional magnetic coupled converters, this paper presents three recently developed multilevel voltage source converters: (1) diode-clamp, (2) flying-capacitors, and (3) cascaded-inverters with separate DC sources. The operating principle, features, constraints, and potential applications of these converters are discussed. Kang and Hyun (2010) proposed a simplified method to calculate the relation between the reference phase voltage and the output phase voltage to the load neutral point. Boora *et al.,* (2010) proposes a new single inductor multi output DC/DC converter that can control the dc link voltages of single-phase diode-clamped inverter asymmetrically to achieve voltage quality enhancements. Namei *et al.,* (2011) developed a hybrid cascaded converter topology with series connected symmetrical and asymmetrical diode clamped H-bridge cells. Pereda and Dixon (2011) suggested a solution for using only one dc source in asymmetric cascaded multilevel inverter. Najafi and Yatim (2012) developed a new multilevel inverter which is used to reduce complexity and gate circuit. Kangarlu *et al.,* (2012) proposes a new topology with reduced number of switches which is used to operate in high power, high voltage, improved output waveform quality and flexibility. Judi and Nowicki (2013) propose bypass technique for multi level inverter to ensure even power distribution in all voltages sources. Kangarlu and Babaei (2013) developed an optimal structure in different criteria such as number of switches, standing voltage on the switches, number of dc voltage sources etc. Babaei *et al.,* (2014) proposed anew algorithm to determine magnitude of dc voltage source. Palanivel and Dash (2011) developed using carrier pulse width modulation technique which is used for lower magnetic interference and high output voltages. Babaei *et al.,* (2015) introduced a new single-phase cascaded multilevel inverter is proposed. This inverter is comprised of a series connection of the proposed basic unit and is able to only generate positive levels at the output.

Cascaded Multilevel Inverter

The main feature of a MLI is its ability to reduce the voltage stress on each power device due to the utilization of multiple DC sources. Though there are several types of MLI, the configuration of MSMI also called cascaded type is unique when compared to other types of multilevel inverter in the sense that it consists of several modules that require SDCS. The function of this MLI is to synthesize a desired voltage from SDCS which may be batteries, fuel cells or solar cells. The number of modules (M) which is equal to the number of DC sources required depends on the number of levels (m) in the output of the MSMI. M and m are related by m=2M+1. For output voltage consisting of five levels, which are $+2V_{dc}$, $+V_{dc}$, 0,$-V_{dc}$ and $-2V_{dc}$, the number of modules required in the MSMI is two. Compared to other types of MLI, the MSMI requires less number of components with no extra clamping diodes or voltage balancing capacitors that only further complicate the overall inverter operation. Each module of MSMI has the same structure whereby it is represented by a single phase full bridge inverter. This simple modular structure not only allows practically unlimited number of levels for the MSMI by stacking up the modules but also facilitates its packaging.

The cascaded MLI can be used as compensator in power systems because it does not present unbalance problem in DC source. The structure of separate DC sources is well suited for various renewable energy sources such as fuel cell, photo voltaic cell and biomass cell.

Figure 1 shows a single phase five level configuration of MSMI. It consists of two H-bridge inverters referred to as MSMI modules that are connected in series to generate five level output voltage. The output voltage of chosen MSMI (Figure 1) is equal to the summation of the output voltages of the respective modules i.e.

$V_o=V_{a1}+V_{a2}$

where V_{a1} - output voltage of module 1 and V_{a2} - output voltage of module 2.

Each module has its own DC source and consists of four power devices designated as S_{11}, S_{21}, S_{31} and S_{41} for the first module and as S_{12}, S_{22}, S_{32} and S_{42} for the second module (Figure 4.5).

Each MSMI module can generate three level of output namely $+V_{dc}$, 0 and $-V_{dc}$. This is made possible by connecting the DC source sequentially to the AC load via the four power devices.

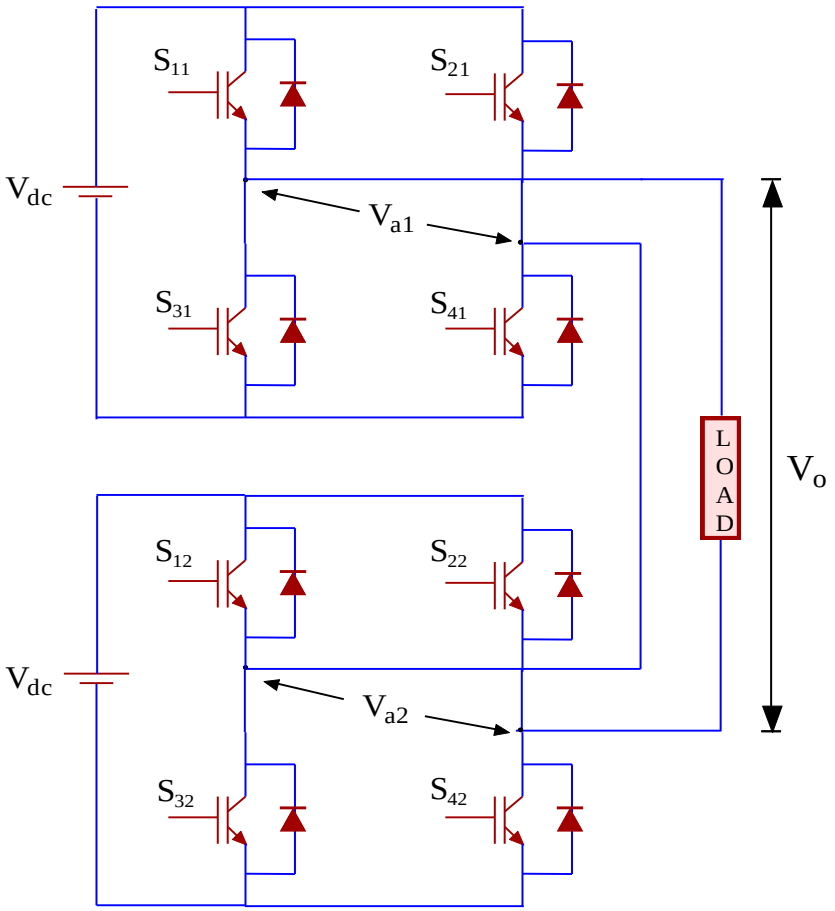

Figure 1: A Single Phase Cascaded Multilevel Inverter

Table 1 lists the output voltage with the corresponding switching states of the upper power devices of the two modules of the five level inverter. As depicted from Table 1, sixteen legal configurations of device switching states and output voltage levels are available for a five level MSMI. From the sixteen configurations available, only five switching configurations are needed for the above MSMI in which the voltage across the each device is V_{dc} or ½ of the peak output voltage. Figure 2 shows the cyclic switching sequence for the chosen MSMI. Figures 4.7 (a), (b), (c), (d) and (e) show respectively the switching strategies to synthesize $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$ at output. Figure 3 shows the operating modes of the single phase five level cascaded inverter.

Table 1: % Switch states and voltage levels of five level cascaded inverter

S_{11}	S_{21}	S_{12}	S_{22}	Output (V_o)
1	0	1	0	$+2V_{dc}$
1	0	0	0	$+V_{dc}$
1	0	1	1	$+V_{dc}$
0	0	1	0	$+V_{dc}$
1	1	1	0	$+V_{dc}$
0	0	0	0	0
1	1	1	1	0
1	0	0	1	0
0	1	1	0	0
0	0	1	1	0
1	1	0	0	0
0	1	1	1	$-V_{dc}$
0	1	0	0	$-V_{dc}$
1	1	0	1	$-V_{dc}$
0	0	0	1	$-V_{dc}$
0	1	0	1	$-2V_{dc}$

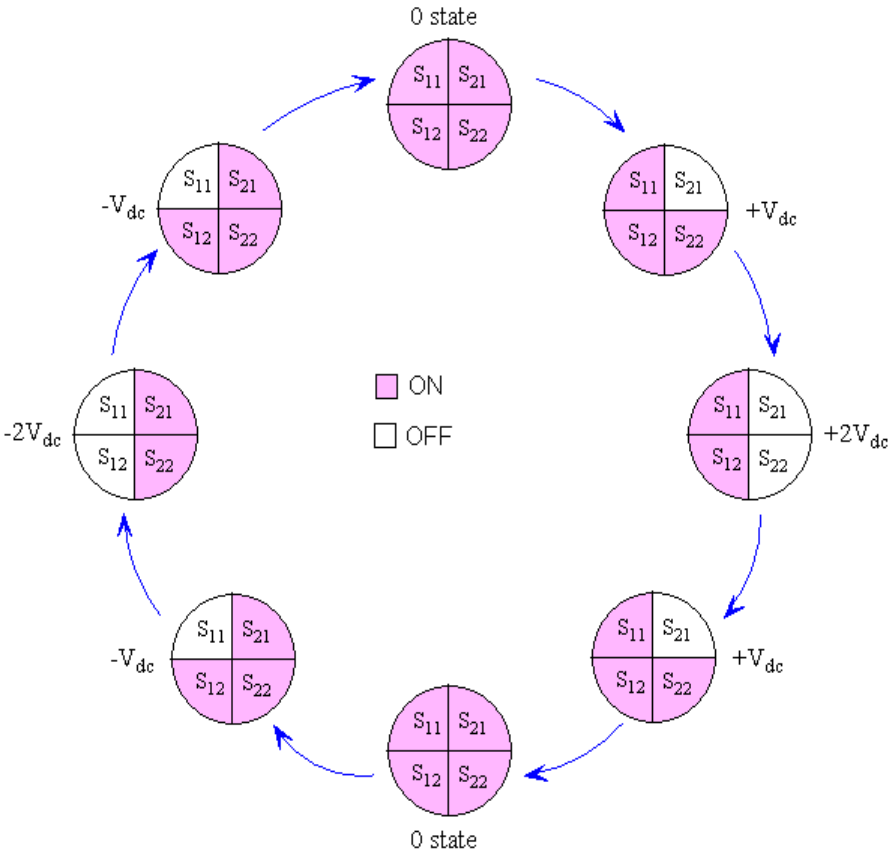

Figure 2: Cyclic switching sequence of chosen MSMI

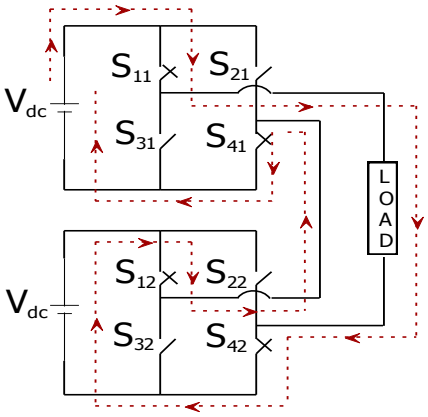

Figure 3: (a) Switching strategy to generate $+2V_{dc}$ at load

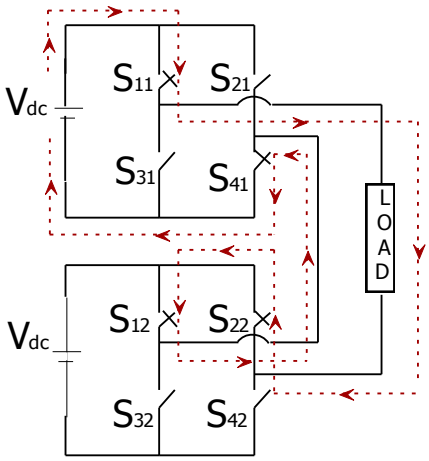

Figure 3: (b) Switching strategy to generate $+V_{dc}$ at load

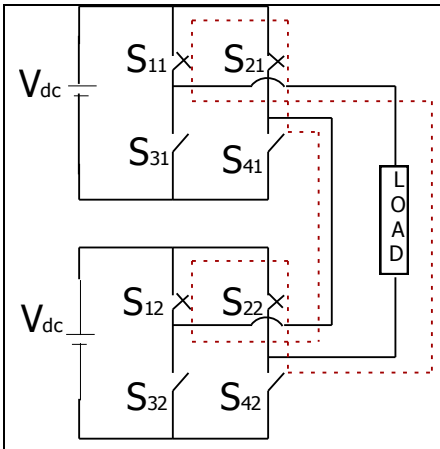

Figure 3: (c) Switching strategy to generate 0 V at load

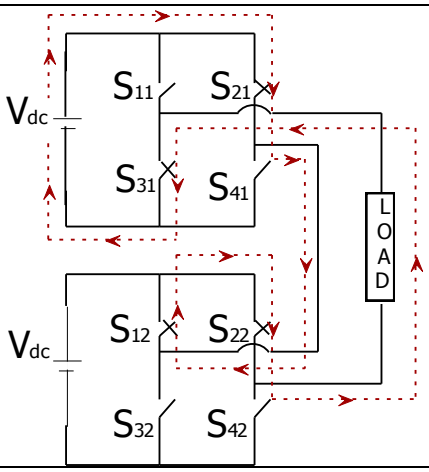

Figure 3: (d) Switching strategy to generate $-V_{dc}$ at load

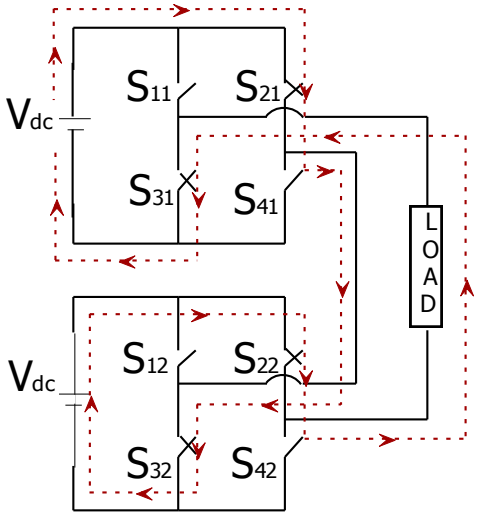

Figure 3: (e) Switching strategy to generate $-2V_{dc}$ at load

Figure 3: Switching strategies for five level cascaded inverter

Modulation Strategies of MLI

PWM techniques are employed in inverters to achieve high quality output voltage of desired amplitude and frequency which are as close as possible to sinusoidal wave. Any deviation from the sinusoidal wave shape will result in electromagnetic interference, harmonic losses and torque pulsation in case of motor drives. The quality of the output waveform will improve with increase in switching frequency**.** It is generally accepted that the performance of an inverter, with any switching strategies, can be related to the harmonic contents of its output voltage. Higher switching frequency can be employed only for low power levels as the switching losses increase with frequency**.** Power electronics researchers have many control techniques to reduce harmonics in such cases. In multilevel inverter technology, there are several well-known low switching frequency modulation topologies out of which the present work focuses on optimized harmonic stepped-waveform technique. Figures 4 and 5 shows the sample carrier arrangement for triangular and random pulse width modulation with sinusoidal reference.

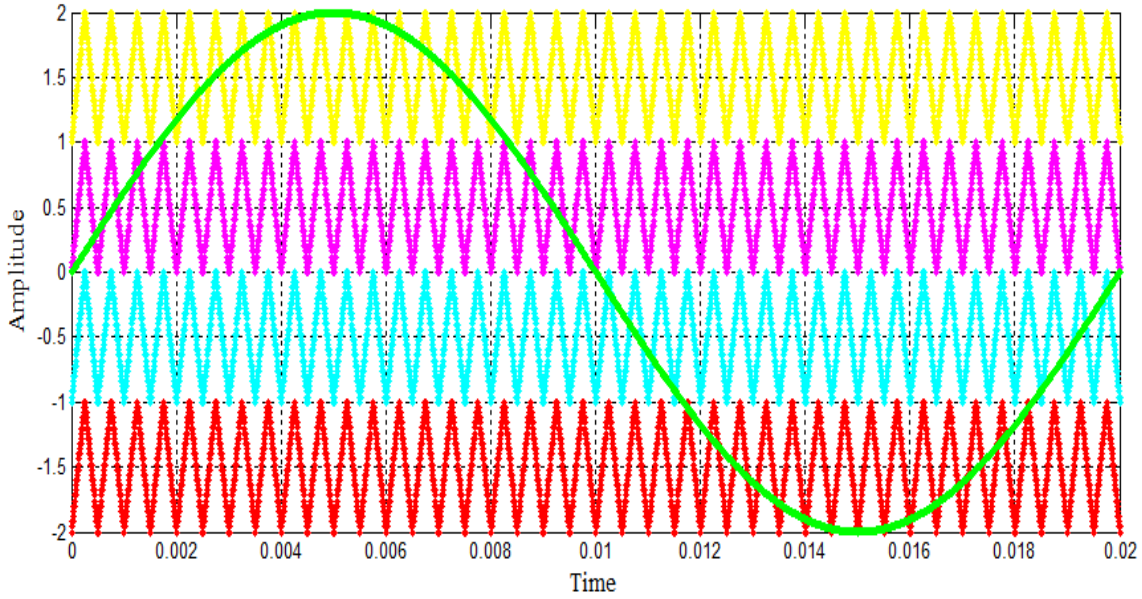

Figure 4: Sample Carrier arrangement for triangular carriers and sine reference

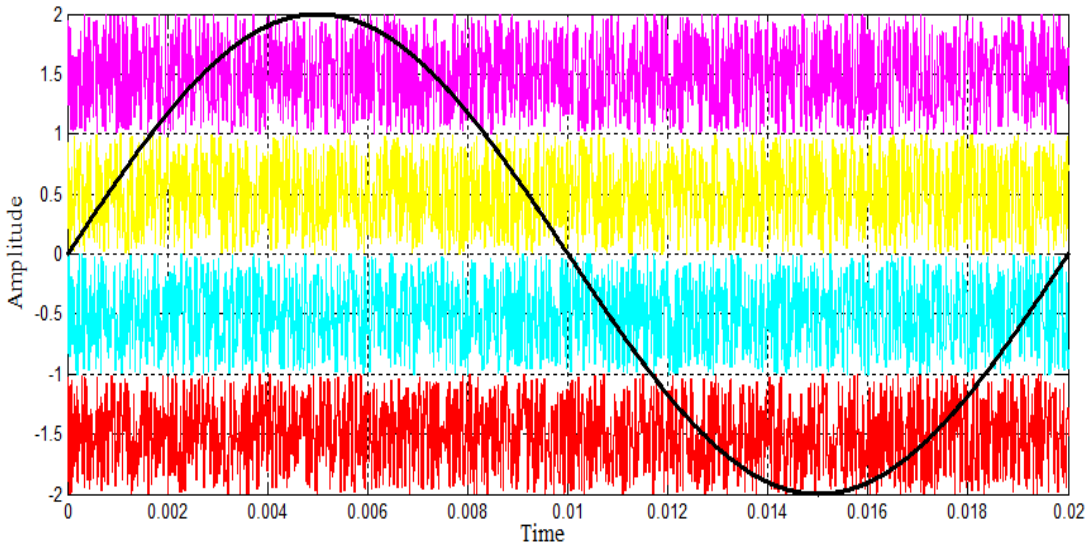

Figure 5: Sample carrier arrangement for random pulse width modulation

Simulation Results

The chosen topology of five level inverter is simulated using SIMULINK - power system block set. Simulations are performed with different values of m_a ranging from 0.6 to 1 and resistive load of 100Ω. Simulated output voltages of chosen MLI with various PWM strategies are displayed only for a sample value of m_a= 0.8. In this section, m_f is chosen as 40 as a trade off in view of the following reasons: (i) to reduce switching losses (which may be high at large m_f) (ii) to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies (iii) to effectively utilize the available FPGA system for hardware implementation. The simulated output voltages are also shown for only one sample value of m_a=0.8. The following parameter values are used for simulation: V_{dc} = 220V and R(load) = 100Ω, f_c = 2000 Hz, f_m = 50 Hz and m_f = 40. Figure 6 and 7 shows the sample output voltage waveform and FFT plot for RPWM technique. Tables 2 and 3 shows the simulated THD and output voltage for various PWM techniques and modulation indices.

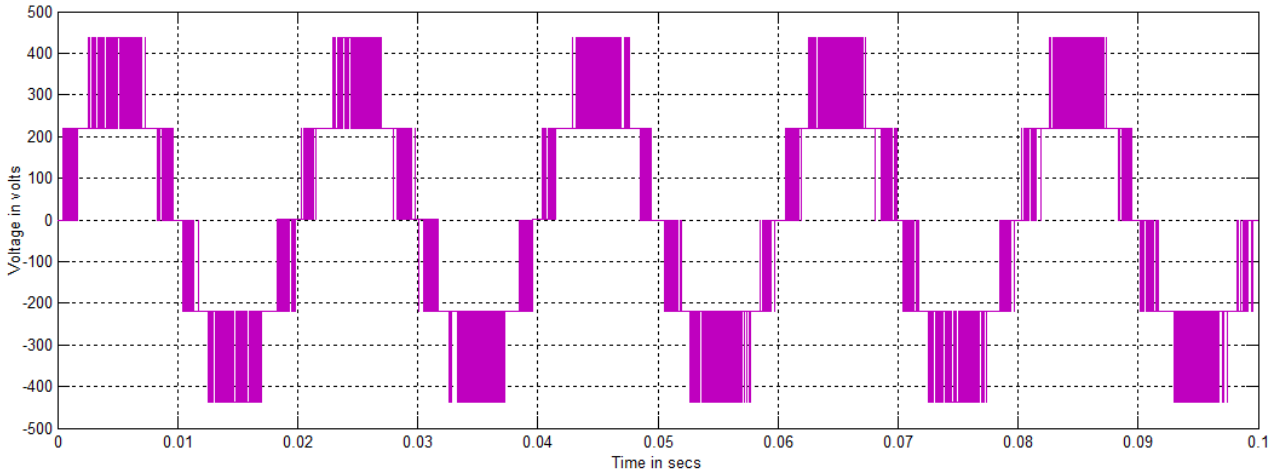

Figure 6: Sample output voltage for random pulse width modulation (m_a =0.8)

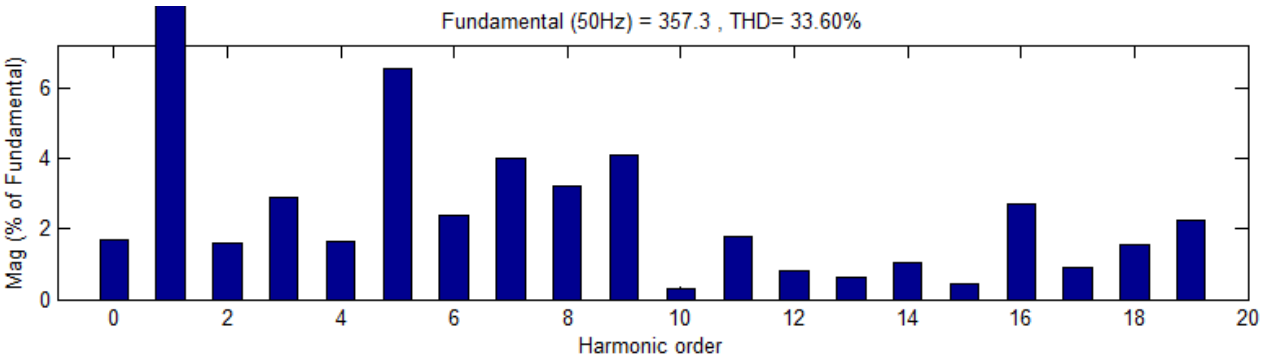

Figure 7: Sample THD plot for random pulse width modulation (m_a =0.8)

Table 2: % THD for different modulation indices for various technique (By simulation)

m_a	PD	POD	APOD	RPWM
1	27.04	26.94	26.52	21.51
0.9	33.62	33.5	33.21	25.98
0.8	38.67	38.12	38.14	33.60
0.7	42.07	41.88	41.97	37.13
0.6	44.47	44.52	44.56	33.91

Table 3: V_{rms} for different modulation indices (By simulation)

m_a	PD	POD	APOD	RPWM
1	310.7	310.7	311.1	319.6
0.9	280	279.9	280.3	293.6
0.8	248.8	249.2	249	252.7
0.7	217.3	217	217.2	207.5
0.6	186.1	185.7	186	179.4

Hardware Results

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform.

The ability to update the functionality after shipping, partial re-configuration of a portion of the design and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications. Figure 8 shows the entire hardware setup with details as in table 4.3. After suitably scaling down the simulation values, in view of laboratory constraints, the peak-to-peak output voltage obtained experimentally is 60 V. Table 4 shows the chosen hardware parameters. Tables 5 and 6 shows the experimental output voltages and total harmonic distortion for various modulation indices and PWM strategies. Figures 9 to 13 the sample waveforms obtained through power analyzer and Fluke meter.

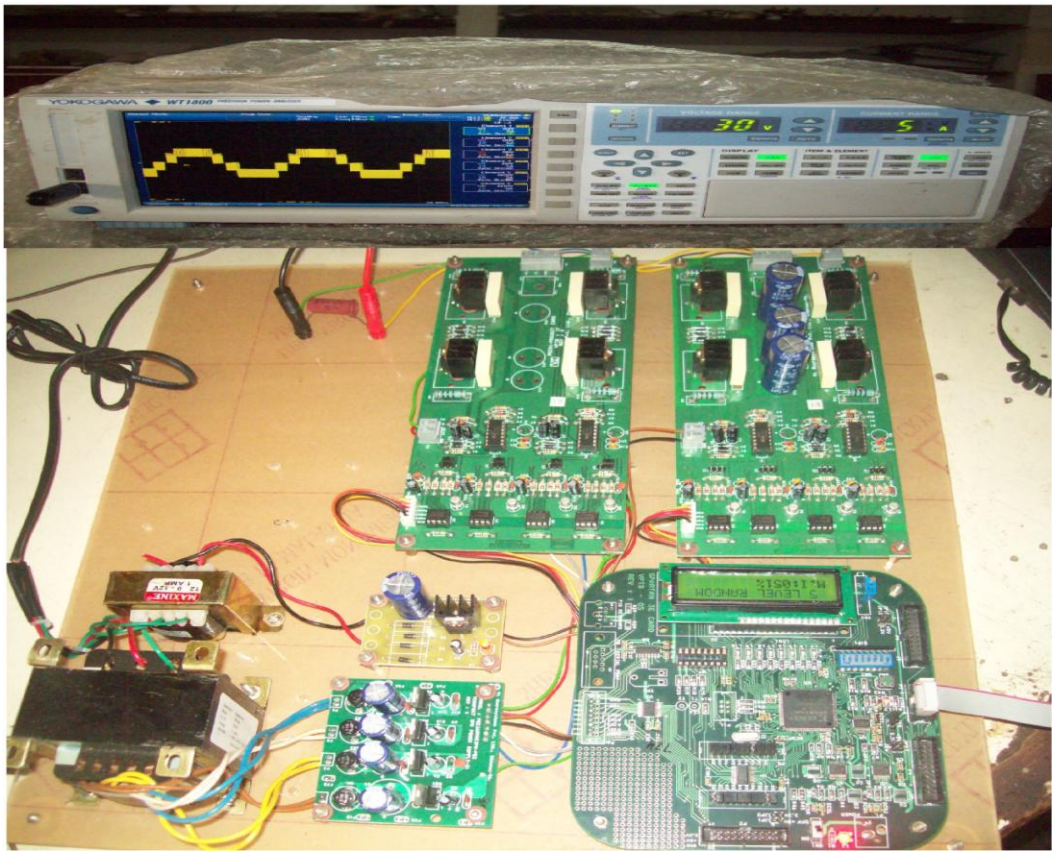

Figure 8: Entire Hardware Setup

Table 4: Hardware Parameters

Parameter	Value
Switching Frequency	3150 Hz
Switching Device	MOSFET
DC Input Voltage	15V-single H-Bridge
Rated Output Frequency	50Hz
Rated output Voltage	60V
R load	500ohm

Table 5: % THD for different modulation indices for various technique (By experimentation)

m_a	PD	POD	APOD	RPWM
1	26.93	28.3	26.93	12.12
0.9	33.41	33.38	33.38	13.9
0.8	38.55	38.56	38.55	16.5
0.7	41.73	41.73	41.73	15.4
0.6	44.43	44.43	44.43	17.9

Table 6: V_{rms} for different modulation indices (By experimentation)

m_a	PD	POD	APOD	RPWM
1	18.86	18.86	18.86	21.25
0.9	16.94	16.94	16.94	20.23
0.8	15.06	15.06	15.06	18.53
0.7	13.24	13.24	13.24	17.34
0.6	11.35	11.35	11.35	15.29

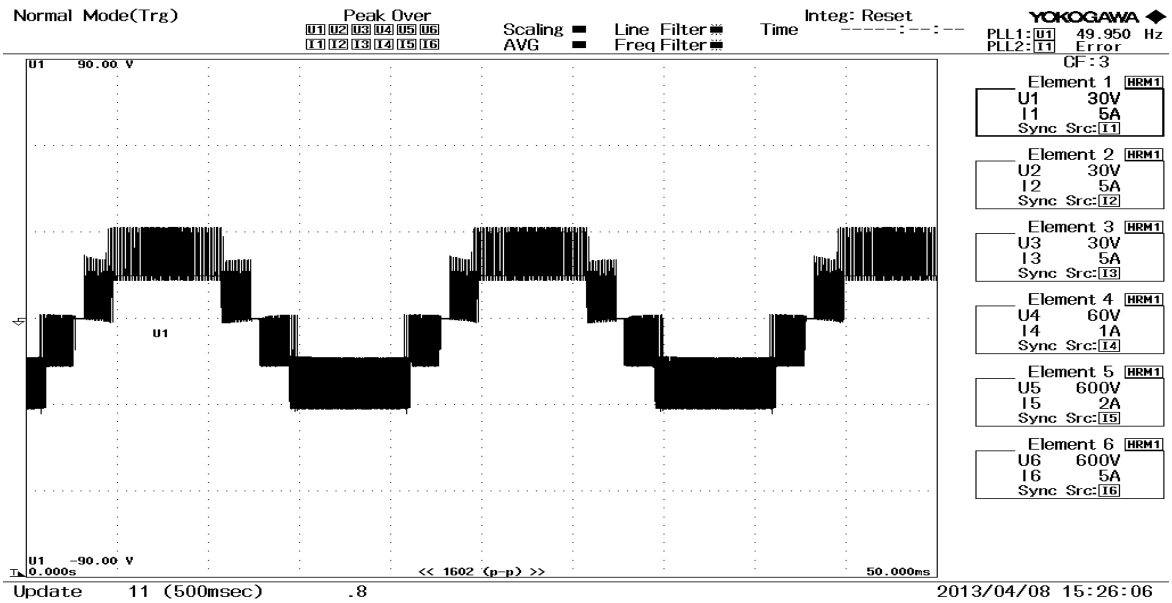

Figure 9: Output Voltage generated by RPWM (m_a = 0.8, m_f = 63)

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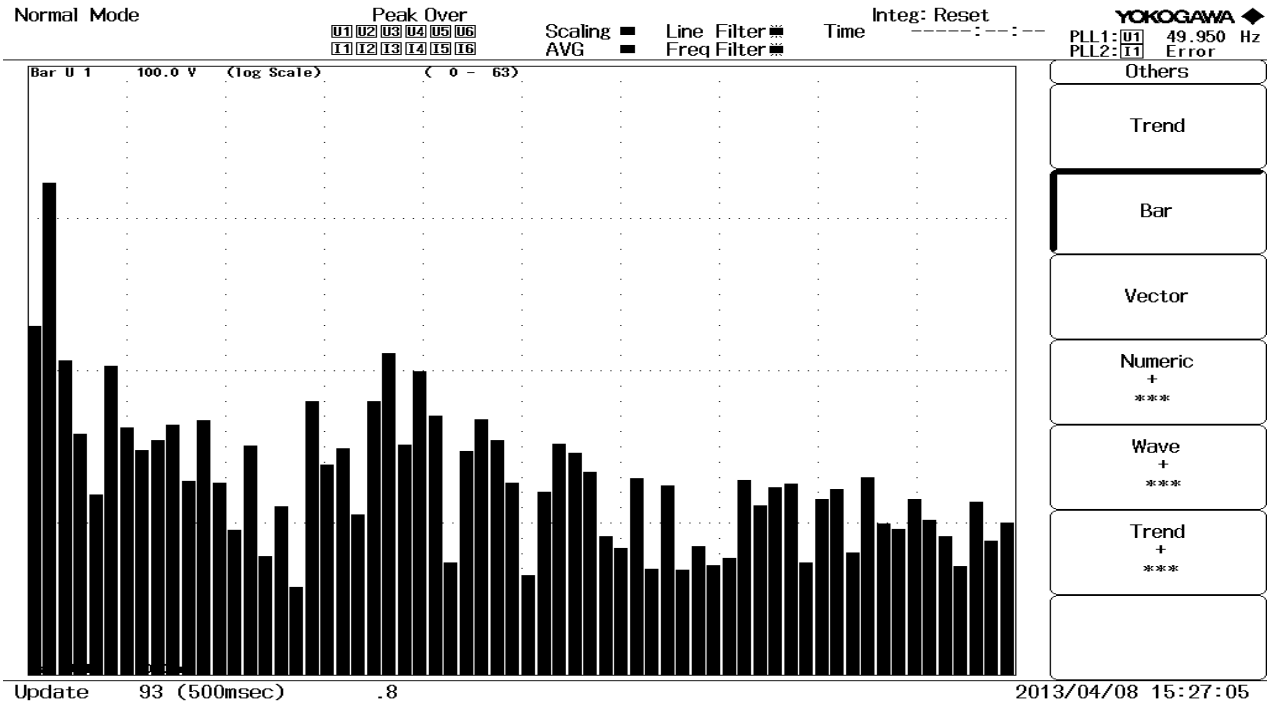

Figure 10: % THD for RPWM strategy (m_a = 0.8 and m_f =63)

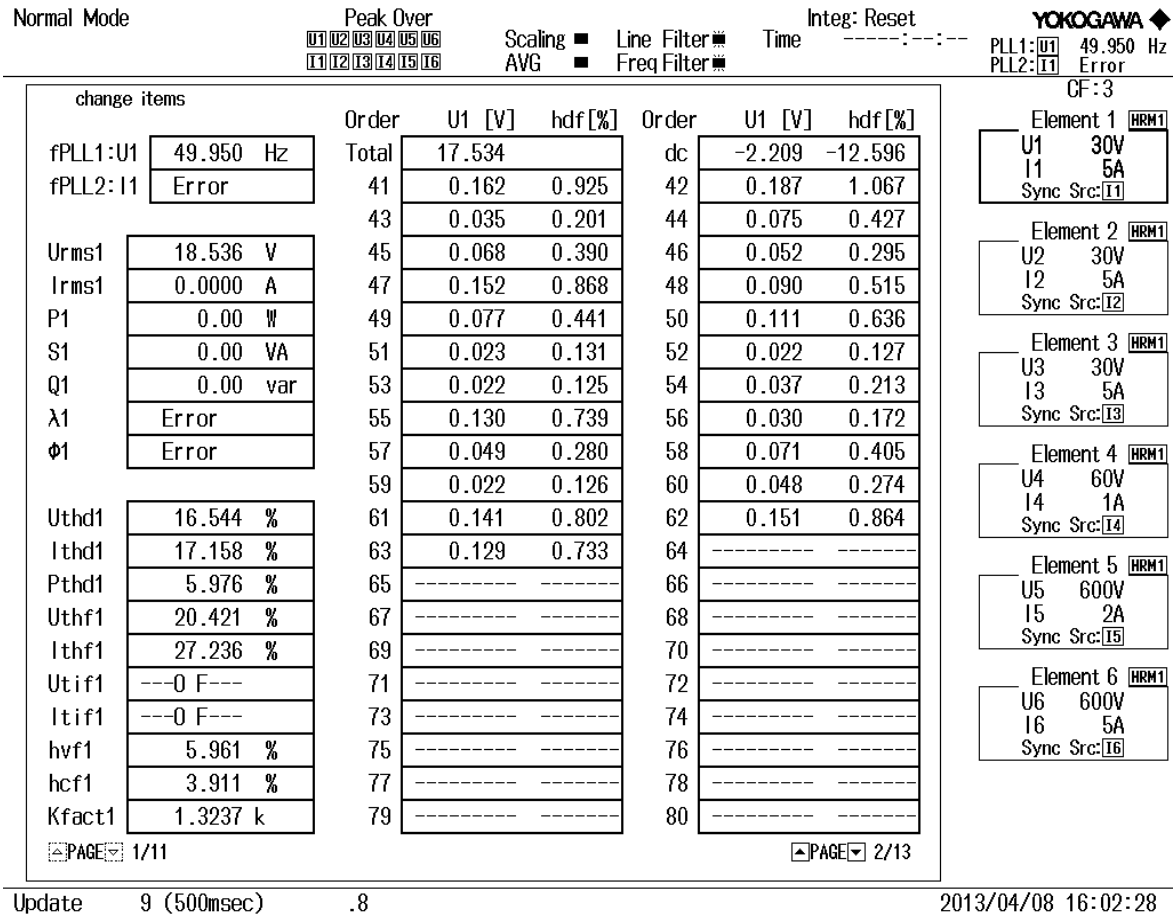

Figure 11: Sample power analyzer output for RPWM strategy (m_a = 0.8 and m_f =63)

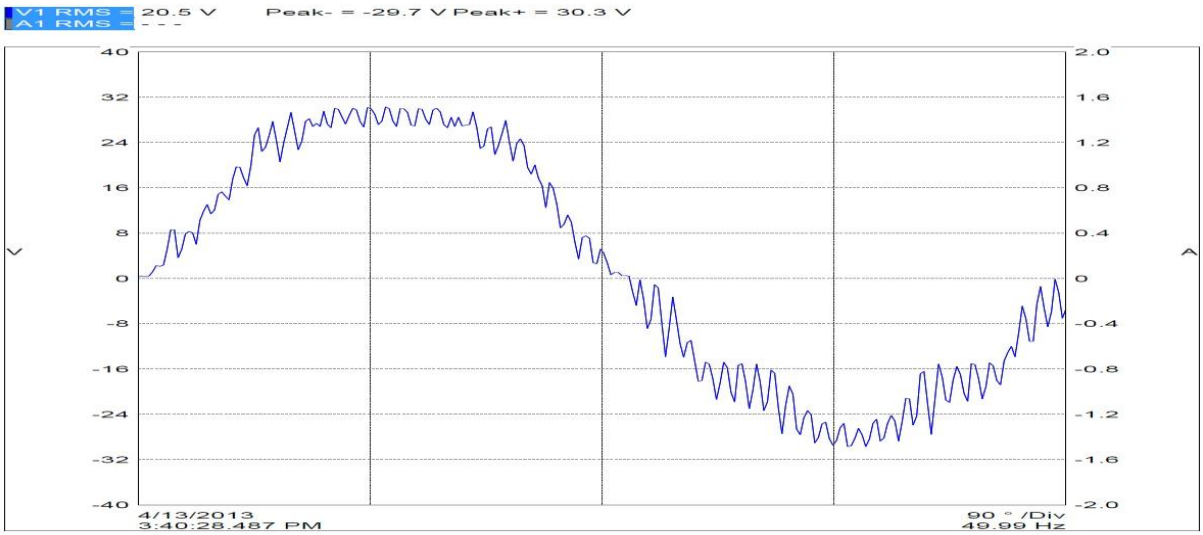

Figure 12: Fluke meter voltage waveform generated by RPWM strategy (m_a -0.8 and m_f =63)

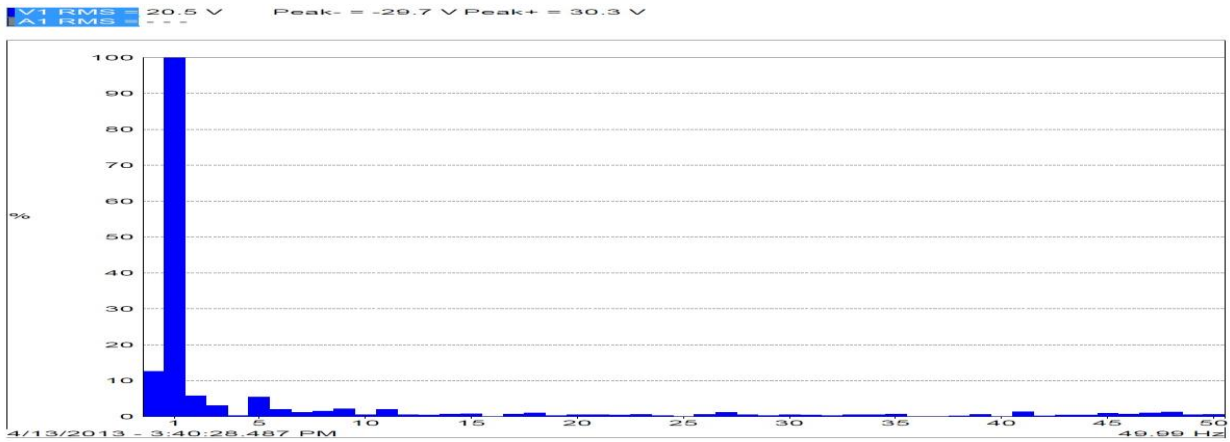

Figure 13: Fluke meter total harmonic distortion waveform for RPWM strategy (m_a - 0.8 and m_f =63)

RESULTS AND DISCUSSION

In this project the simulation results of single phase, five level cascaded multilevel inverter for R-load with various modulating techniques are implemented through MATLAB/SIMULINK. The output quantities like THD spectrum and V_{rms} are obtained. The simulation THD values for the PD, POD and APOD techniques where compared with the calculated THD values by varying the modulation index. The graphical representation shows the nature of the THD values clearly. The obtained THD values are compared with the RPWM technique. Comparing the result, we found that the THD value for RPWM is less that of the Triangular carriers.

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