International Journal of Applied Engineering and Technology ISSN: 2277-212X
An Open Access, Online International Journal Available at http://www.cibtech.org/jet.htm
2022, Vol.12, pp.176-182/Pandiyan et al.
Research Article

DIGITAL CONTROL BASED ASYMMETRIC CASCADED MULTILEVEL INVERTER FOR ELECTRIC VEHICLE

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ABSTRACT
This paper discuss about cascaded H bridge multilevel inverter (CHMLI) has expanded in recent years due to its recompenses in more voltage and more power with less harmonics uses and implemented in micro controller based cascaded multilevel inverter for single phase in Electric vehicles. MOSFET's are used as switching element. In this paper new switching pattern for the cascaded H bridge multilevel inverter. A normal cascaded H bridge multilevel inverter requires N-numbers of DC sources for 2^{N+1} levels of output, where 'N' is the number of inverter steps. Also it present topology to control cascaded inverter that is implemented with several DC sources to get 2^{N+1}–1 levels. This proposed system is implemented by a low cost microcontroller on seven level cascaded H bridge inverter. Several multilevel topologies have been reported in the literature and this paper focuses on digital control of asymmetric cascaded MLI. Gating signals are generated using PIC microcontroller. The performance of the MLI has been analyzed and compared with the results attained from theory. A proposed system based on seven-level inverter, which control the high performance 8-bit normal microcontroller with gate driver circuit, in additional hardware is used, which allows the flexible and cost-effective clarification. The output voltage can be different in a great range and with a better resolution. This combination makes the scheme and analysis of H Bridge multilevel inverter more widespread and in depth.

Keywords: *Multilevel inverter, Flip-flop, Digital control, PIC micro-controller*

INTRODUCTION

In a multilevel inverters, introduced about 20 years before entails execution of power conversion in several voltage steps to obtain better power quality, low switching losses, higher voltage capability and better electromagnetic compatibility [Albert (2009)]. But, the main disadvantages of MLI include disturb voltage problems, unsatisfactory current stresses and higher operation cost. Now a days more topologies of multilevel inverters have been implemented, the most prevalent are flying capacitor, diode clamped and cascaded H-bridge arrangements. One of the most facets is cascaded H-bridge away from each other multilevel inverters is the ability of operating different DC sources on the separate H-bridge cells which consequences in severe the power conversion amongst higher-voltage lower frequency and lower-voltage higher-frequency inverters *[M. Hagiwara,(2010)]*. The advantage of this proposed system is that isolated the sources are not compulsory for separate phase. This paper proposed multilevel inverter containing of series connection of separate three phase or single (full bridge) inverter modules on the AC output terminals. This topology is suitable for applications where separate DC voltage sources are available, such as photovoltaic generators, fuel cells and batteries *[L.M.Tolbert,(1999)]*. To implement cascaded multilevel inverter firing, a sequence is required, which in turn needs microcontroller. Section II discuss about straightforward operation of asymmetric cascaded H bridge multilevel inverter. Section III discusses about the digital control technique with the implementation of microcontroller. Section IV focuses on the simulation results. Section V deals with the conclusions.

CASCADED MULTILEVEL INVERTER

The cascaded H-bridges inverter consists of H-bridges in series configuration. Such technology is very attractive for application such as motor drive systems, power distribution, power quality and power conditioning application *[Jose Rodriguez 2007]*. Each H-bridge inverter module can generate three different output voltage levels namely 0, $+V_{dc}$ and $-V_{dc}$. The multilevel inverter of Fig.l utilizes two independent DC sources and consequently will create an output phase voltage with seven levels. 'N' is the number of independent DC sources per phase, 'm' is the number of levels, 'l' is the number of switches with freewheeling diodes per phase, then the following equations are applied for CMLI :

$m = 2N + 1$ (1)

$l = 2(m - 1)$ (2)

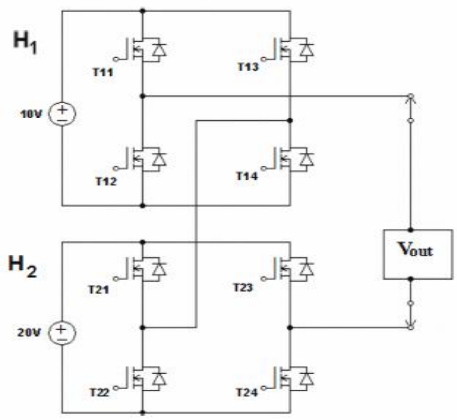

Figure 1: Power circuit of CMLI

A simplified single phase topology is shown in Fig. 1 The output voltage will be + 10V (top inverter H_1) when switches T_{11} and T_{14} conducts. Similarly -10V will be obtained when T_{12} and T_{13} conducts. The output voltage is +20V only when T_{21} and T_{24} are conducting and the output voltage is -20V only when T_{22} and T_{23} are conducting. The output voltage +30V is available when switches T_{11} ,T_{14} ,T_{21} and T_{24} conducts and -30V is available when switches T_{12},T_{13},T_{22} and T_{23} conducts. The first bridge H_1 consists of a separate DC source V_{dc}, whereas the second bridge H2 consists of a DC source $2V_{dc}$ as shown in Fig.1. Let the output of H-Bridge-1 be denoted as $v_1(t)$ and the output of H-Bridge-2 be denoted as $v_2(t)$. Hence the total output voltage is given by $V(t)= V_1(t)+V_2(t)$. By alternately opening and closing the switches T_{11}, T_{14} and T_{12}, T_{13} of H-Bridge- 1 appropriately, output of H_1 $v_1(t)$ can be made equal to $+V_{dc}$, 0 or - V_{dc}. Similarly the output voltage of H-Bridge-2 $v_2(t)$ can be made equal to $-2V_{dc}$, 0 or + $2V_{dc}$ by opening and closing the switches of H_2. Hence v(t) takes values–$3V_{dc}$, $-2V_{dc}$,-Vdc, 0, $+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$ which are the seven levels of inverter output. The output voltage of the cascaded H-Bridge multilevel inverter is by:

$V(t) = V_1(t) + V_2(t)$ ... (3)

i) Harmonics: The switching angles of the waveform will be adjusted to obtain the lowest output voltage THD. The harmonics orders and magnitude are depends up on the type of inverter and the control techniques. For example in single phase VSI, the output voltage waveform typically consists only of odd harmonics. The even harmonics are not present due to the half wave symmetry of the output voltage harmonics. The harmonic spectra depend on the switching frequency and the control method.

ii) Switching control of the inverter: There are number of modulation control techniques such as sinusoidal PWM method (SPWM), space vector PWM method (SVPWM), selective harmonic elimination method (SHE), and active harmonic elimination method, and they all can be used for inverter modulation control*[A.M. Massoud,(2010)]*. For the proposed inverter control, a sensible modulation

control method is the digital switching control for high and lower output voltage. In this paper, digital switching control is used in H-bridge MLI. The multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages in stepped waveform. The commutation of the switches allows the addition of the capacitor voltages which reaches the high voltage level at the output, while the power semiconductors withstand only with reduced voltage. A single phase leg of inverter with different numbers of levels by which the action of the power semiconductors is represented by an ideal switch with several positions*[A.K Sadigh(2010)]*. A seven-level multilevel inverter generates an output voltage with seven values (levels). By considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load k is defined by:

$K = 2m + 1$ … (4)

The number of steps p in the phase voltage of a single phase load in wyes connection is given by:

$p = 2k + 1$ … (5)

The term multilevel starts with the three-level inverter. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveforms, it results to reduction in harmonic distortion*[H.Taghizadeh(2010)]*. However, a high number of levels results to increase the complexity and also it introduce voltage imbalance problems. Three different topologies have been proposed for multilevel inverters as diode-clamped (neutral clamped), capacitor- Clamped (flying capacitors) and cascaded multi cell with separate dc sources*[Nirmal(2020)]*. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: Multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination and space-vector modulation (SVM).

The most attractive features of multilevel inverters are as follows:

1) It can generate output voltage with extremely low distortion.
2) It draws input current with very low distortion.
3) It generates smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, by using sophisticated modulation methods, CM voltages can be eliminated.
4) They can operate with a lower switching frequency.

Table 1: Conduction table for CMLI

Voltage (V)	T_{11}	T_{12}	T_{13}	T_{14}	T_{21}	T_{22}	T_{23}	T_{24}
-30V	0	1	1	0	0	1	1	0
-20V	0	0	0	0	0	1	1	0
-10V	0	1	1	0	0	0	0	0
0V	1	1	1	1	0	0	0	0
+10V	1	0	0	1	0	0	0	0
+20V	0	0	0	0	1	0	0	1
+30V	1	0	0	1	1	0	0	1

DESIGN AND DISCRIPTION OF FLIP-FLOP TECHNIQUE

In figure-2 shows the hardware implementation of digital control technique, PIC16F874A/877A micro controller is used to control the MOSFETs. PIC16F series microcontroller which is used for this paper, a 40-pin device, 8 bit CMOS Microcontroller which belongs to the MICROCHIP family of microcontrollers. It has 10-bit Analog to Digital converter (ADC) and we have used only 8 bits for our control so that the speed can be controlled in 255 steps ranging. The various features of this device make this device to be selected for the proposed control. Timer1 is operated in external oscillator mode with an external crystal oscillator of 20 MHz connected to the micro controller device. An external Potentiometer is connected to the ADC pin which provides the required speed range.

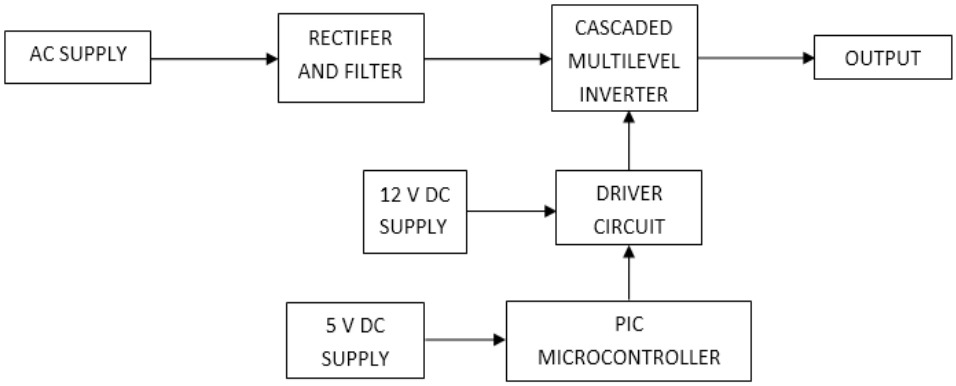

Figure 2: Block diagram of Microcontroller based control of CMLI

SIMULATION CIRCUIT AND RESULT

In figure 3 shows the schematic diagram of digital control technique of cascaded multilevel inverter. In a proposed system two H-bridge multi level inverter is design and flip-flop is used to generate the gate pulses, that gate pulses passing through the various MOSFET terminals. In this design AND gate and OR gates are used. Finally bridge1 and bridge 2 output voltage is connected to load terminal.

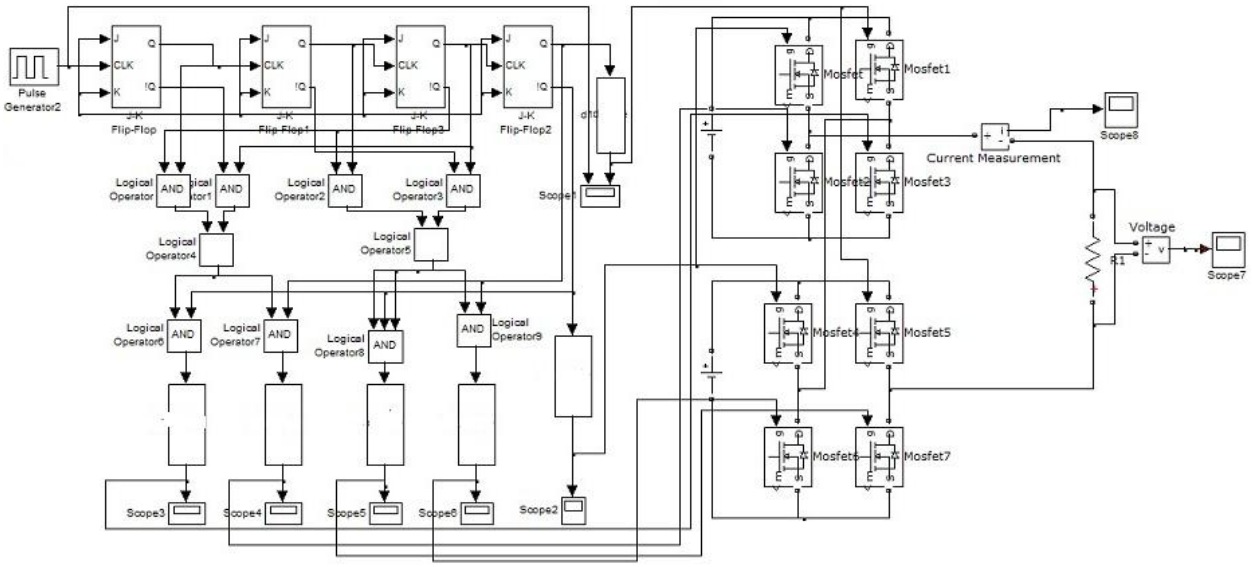

Figure 3: Simulation diagram for proposed method

Gating Pattern of Switches

The below figure 4 shows the various gate pulses of digital control technic. Amplitude of the all the gate signal is 1 Volt and phase angle is different.

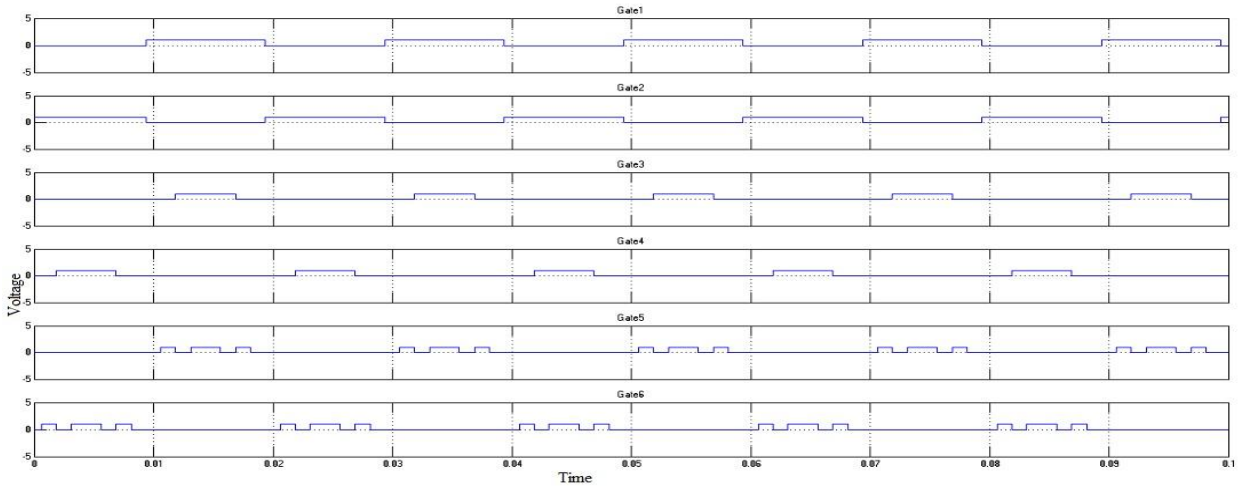

Figure 4: Gate Pulses of various switches

RESULT AND DISCUSSION

Simulation circuit of the cascaded multilevel inverter implemented and the output waveform is shown in figure 5. In this proposed system output is 7-level, for x-axis time(ms) is taken and y-axis is output voltage(volt) is taken. The output of this system is 30V and RMS voltage of the system is 18.79 Volts. In figure 6 Total harmonics destruction is analysis by using FFT analyzer, this part %THD value is 21.79%.

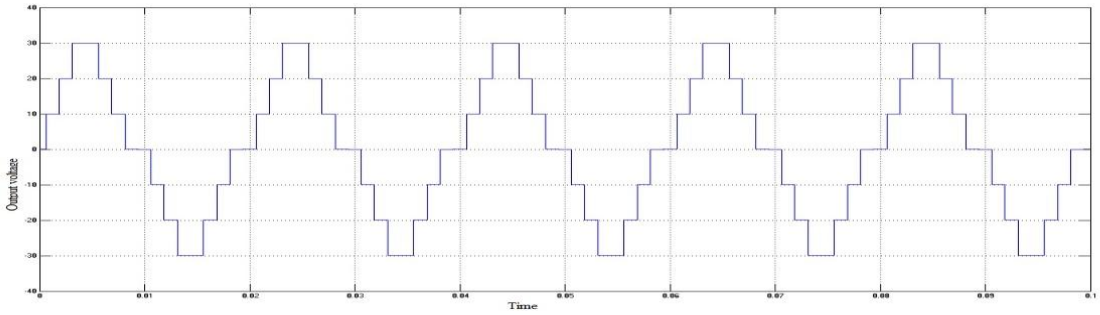

Figure 5: Seven level output of Multilevel Inverter

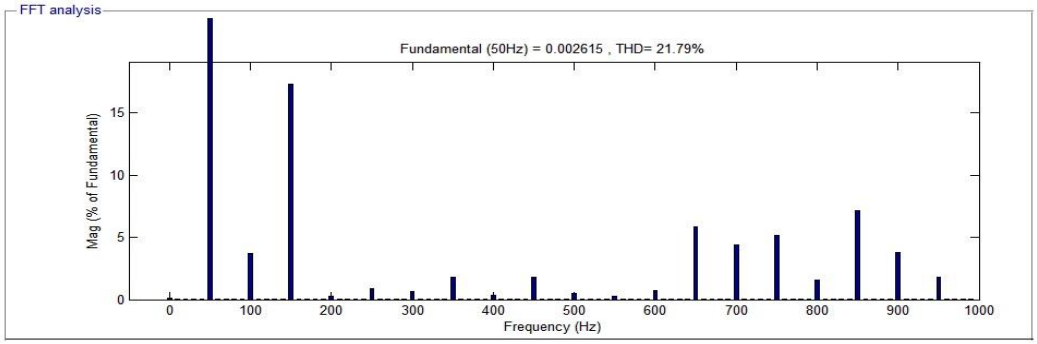

Figure 6: FFT analysis of CMLT

HARDWARE IMPLEMENTATION

Simulation of cascaded multilevel inverter output voltage is verified by single phase hardware prototype, which includes eight MOSFET switches. This cell consists of two power stages by an asymmetrical DC sources. In each power stage, four MOSFETs are used. A PIC 16F877 microcontroller is used as the main processor, which provides gate logic signals. This signals used to control the MOSFET switches for ON and OFF conditions and generate the step waves. The output terminal of the inverter is connected to electric vehicle drives. The proposed block diagram is shown in Figure 2. And result is exposed in the resultant voltage.

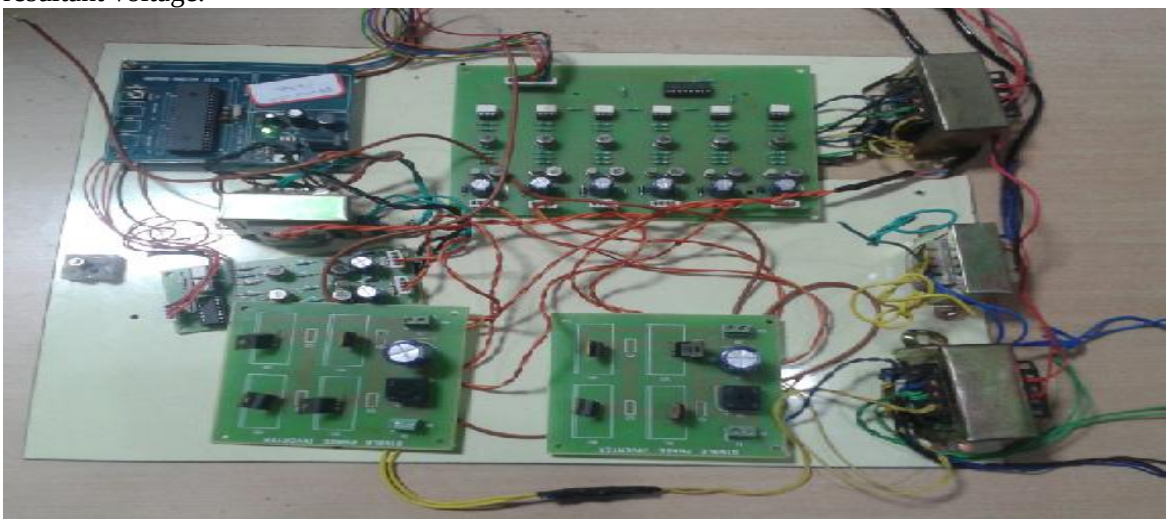

Figure 7: Experimental overview of CMLT

In the driver circuit, low power components are used like IR2101 ICs and connected to MOSFET switch's .

Hardware output of Multi level inverter:

The below figure 8 shows the output voltage of seven level inverter. Output voltage in Volts is taken in y-axis and time in milliseconds is taken in x-axis. By using CRO to measure the waveform of output voltage and the hardware output voltage is 30V.

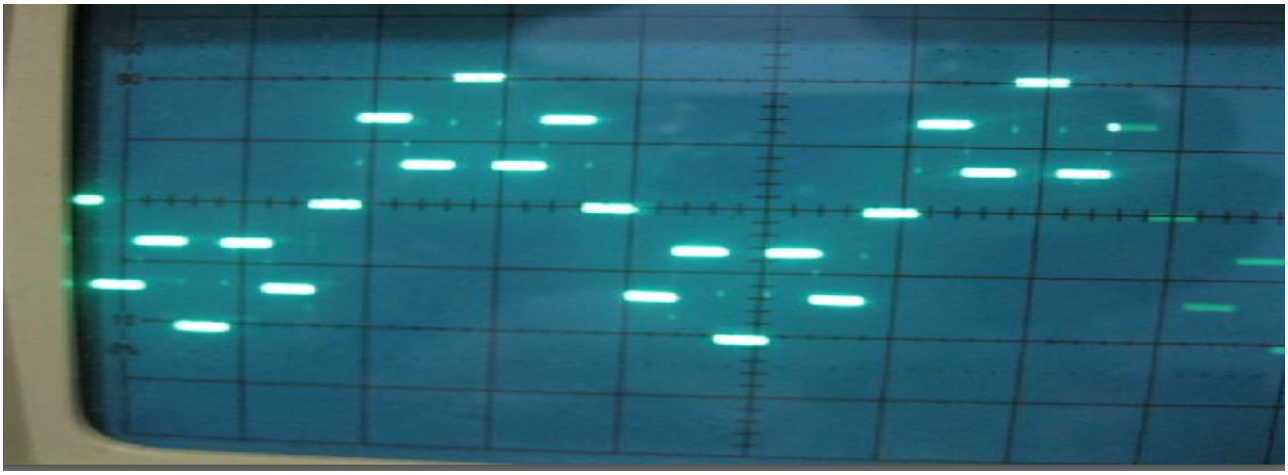

Figure 8: Seven level hardware output of Multilevel Inverter

CONCLUSION

In cascaded H-bridge multilevel inverter separated unequal DC sources are used to generate sinusoidal output. A digital switching scheme is used and produces a nearly sinusoidal output. This cascaded inverter design is to get the improved sinusoidal output of an inverter and gives less THD%. The elimination of harmonics in a cascade H bridge multilevel inverter by considers the inequality of separated dc source. A Micro-controller based gating circuit generates the pulses required to the inverter. This can be important in the high power quality cascaded multilevel inverters which require several voltage sources and knowledge of the dc voltage levels. Applications of the cascaded multilevel inverter include Naval ship propulsion which necessitates high power quality. The proposed solution was based on a high performance 8- bit microcontroller with gate driver circuit and additional hardware.

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