Indian Journal of Fundamental and Applied Life Sciences ISSN: 2231– 6345 (Online)
An Open Access, Online International Journal Available at www.cibtech.org/sp.ed/jls/2014/03/jls.htm
2014 Vol. 4 (S3), pp. 442-453/Gholamrezaei et al.
Research Article

A NOVEL CNTFET CIRCUIT DESIGN TECHNIQUE TO IMPLEMENT KLEENE'S THREE-VALUED LOGIC

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ABSTRACT
Recently, Multiple-Valued Logics (MVLs) has found a significant role in the Integrated Circuits' world. By using these logics, we can achieve a higher circuit density while performing more complex operations with less interconnection problems. Since the most MVLs are derived from ternary logics, implementations of three-valued systems are very important. One of the most significant ternary logics is Kleene's three-valued logic. By Using Carbon Nanotube Field Effect Transistors (CNTFETs), we can achieve multiple threshold voltage levels which make them ideal for implementing Kleene's three-valued logic. In this paper, we have used a novel design technique based on CNTFETs to implement the basic functions of Kleene's logic. This new technique empowers us to design high performance circuits with lower power consumption, which occupy smaller area as well. In addition, we have optimized these circuit designs in power consumption and propagation delay. Simulation results using Synopsis HSPICE show the accuracy of our optimizations.

Keywords: *MVL, Kleene's Three-Valued Logic, CNTFET*

INTRODUCTION
The last few years attested a considerable increase in nanotechnology researches, especially the nanoelectronics (Yao 1999). Carbon nanotube field effect transistor has significant potential to replace MOSFET technology in the future due to unique mechanical and electrical properties. Now in order to sustain Moore's law and to ensure further improvement in FET performance, it is necessary to look for an alternative like CNTFETs that promise to deliver much better performance than existing MOSFETS. CNTFET technology can also be easily matched with the bulk CMOS technology on a single chip and utilize the same infrastructure (Yao, 1999; Li, 1996). Compared to binary logic, the multiple-valued logic circuit provides better performance in chip size, speed, a small number of interconnections also we have a simpler realization of logical functions (Mukaidono 1986). In the last decades, because of all the multiple-valued logic circuit designs benefits considerable attention have been shown. MVL circuits have more than two logical levels and depending on the number of levels, we may have a ternary (base=3) or quaternary (base=4) logic styles (Wu 1990).

In CNTFETs, the threshold voltage of the transistor is established by the diameter of the carbon nanotubes (CNTs). Therefore, a multiple-threshold design can be achieved by employing CNTs with different diameters (which will be controlled by chirality) in the CNTFETs. This quality makes CNTFETs ideal for bringing MVLs on electronic chips (Raychowdhury 2005).

Many MVLs such as Galois, LukaSiewicz, Literal and Godel have already been efficiently implemented by CNTFETs (Keshavarzian 2009, Keshavarzian 2012, Keshavarzian 2007, Keshavarzian 2009, Keshavarzian 2012). On the other hand, Kleene's three-valued logic is among the best-known and best-motivated of the multiple-valued logics (Fitting 1991). Therefore, implementation of Kleene's logic using CNTFETs can be a very good breakthrough in MVL circuits' world. We have used a new method of CNTFET circuit design which lets us omit the resistors in our circuits (LIN 2009).

This paper begins with an introduction of CNTFETs in section 2. Afterwards, an introduction of Kleene's three-valued logics is presented in section 3. Section 4 is dedicated to our designs and simulation results. Finally, in section 5, the experimental results and optimization of dynamic parameters are presented.

Research Article

Carbon Nanotube Field Effect Transistor

Carbon nanotube field effect transistors are a propitious technology, which have been replaced with primitive silicon devices. A field-effect transistor (FET) based on a single wall carbon nanotube (SWCNT) was successfully fabricated and demonstrated to be able to operate at room temperature at 1991 (Iijima 1991). Carbon nanotube field-effect transistors (CNTFETs) have attracted significant interest as the next-generation devices for nanoelectronics (Tans 1998).

Figure 1(a) illustrates one-dimensional conductor named single walled carbon nanotube (SWCNT) that can be either metallic or semiconducting depending upon the arrangement of carbon atoms defined by their Chirality, C_h (i.e. The direction in which the graphite sheet is rolled) whose magnitude with CNT diameter (D_{CNT}) is given by Eq. 1 and Eq. 2 respectively, where 'a' is the graphite lattice constant (0.249 nm) and n_1, n_2 are positive integers that specify the chirality of the tubes. SWCNT can be supposed as a sheet of graphite which is rolled up and joined together along a wrapping vector (Eq. 1)**,** as shown in figure 1 (b), where a_1, a_2 are unit vectors (Iijima 1991, Tans 1998). The CNT is called zigzag, if n_1= 0, armchair, if n_1= n_2, and chiral otherwise.

$$C_h = \sqrt{n_1.a_1 + n_2.a_2} \qquad \text{(Eq.1)}$$

$$D_{cnt} = C_h / \pi \qquad \text{(Eq.2)}$$

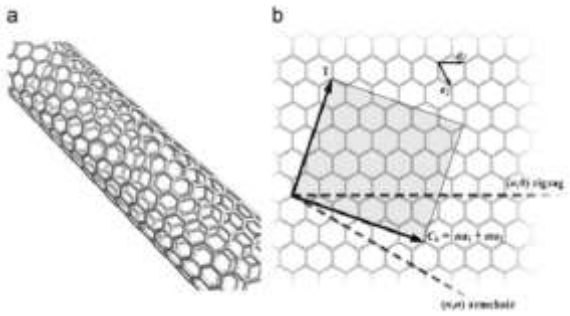

Figure 1: (a) SWCNT (b) Graphite sheet in terms of chirality n1 and n2

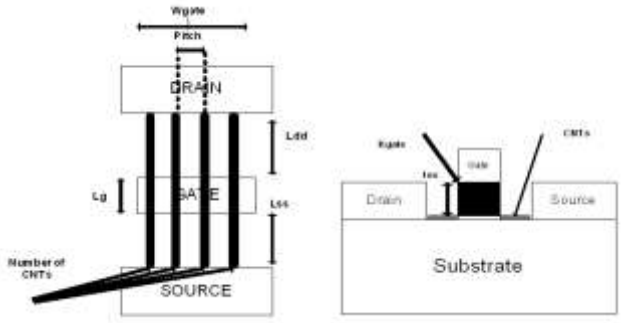

Figure 2: Schematic CNFET cross-section

Substituting the channel of a conventional MOSFET by a number of semiconducting carbon nanotubes is one of the particular details in CNTFET as shown cross-section in figure 2 (McEuen 2002). The major operation of CNTFET is the same as traditional MOSFET. Since the electrons are only limited to the narrow nanotube, the mobility goes up substantially on account of ballistic transport as compared with the bulk MOSFET (Avouris 2004).

There are two types of carbon-nanotube transistors that are being extensively studied. One is a tunneling device figure 3(a) that works on the principle of direct tunneling through a Schottky barrier at the source–channel junction.

The barrier width is modulated by application of the gate voltage so that the trans-conductance of the device is dependent on the gate voltage (Hwang 2008). To overcome these disadvantages associated with Schottky barrier CNTFETs, there have been attempts to develop CNTFETs which would behave like normal MOSFETs. These attempts have met significant success so far with an enormous potential. The MOSFET-like CNTFET (figure 3 (b)) operates on the principle of barrier height modulation by application of the gate potential. In this paper, we will consider the non-Schottky-barrier MOSFET-like unipolar CNTFET with ballistic transport as our device of interest.

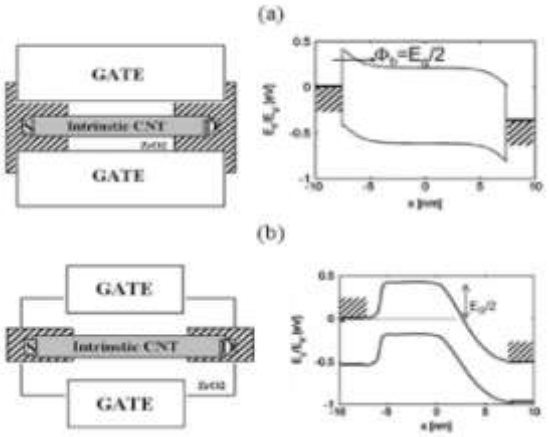

Figure 3: Two type of single walled CNTFETs (a) Schottky barrier, (b) MOSFET-like

Hereafter in this paper the abbreviation CNTFET will be used to denote such a MOSFET-like device unless otherwise stated (figure 3 (b) shows the band diagram of this device) (Hwang 2008, Pourfath 2005, Guo 2003).

The source Fermi level for a degenerately doped source can be derived from the conduction band edge. Inside the intrinsic channel, the Fermi level is in the middle of the band-gap. An important property of these CNTFETs is that the band-gap is inversely proportional to the diameter of the nanotube as Eq. 3 (Tans 1998).

$$E_g = \frac{0.84}{d(nm)} ev \qquad \text{(Eq. 3)}$$

$$V_{th} = \frac{0.42}{d(nm)} ev \qquad \text{(Eq. 4)}$$

As the barrier height determines the threshold potential of a FET, the threshold voltage of the CNTFETs can be expressed as Eq.4.

This geometry-dependent threshold voltage has been exploited in this study to obtain CNTFETs that turn on at different voltages depending on their diameters. It is worth mentioning that the circuit realization of the ternary logic family involves dual- transistors. CNTFETs provide an opportunity to obtain two functional behaviors by using two different tube diameters. CNTFETs provide the unique opportunity of being controlled by changing the carbon nanotube diameter. Therefore, in this paper, we have used a dual-diameter CNTFET-based design for the ternary logic implementation to present TVL (ternary valued logic) Kleene field circuit design.

Kleene's Three-Valued Logic

MVL circuits can reduce the number of operations necessary to implement a particular mathematical function and further, have an advantage in terms of reduced area. In comparison to the fastest binary counterpart, Chip area and power dissipation have been shown to be reduced using efficient MVL implementation 3, (Wu 1990).

Research Article

Ternary logic gets special attention among Multiple Valued Logics (MVLs). MVL is an alternative to common practice binary logic, that most of them have been expanded from ternary (three valued) logic. By adding on a third value to the binary logic, we have ternary logic functions which are significant. In this paper, 0, 1, and 2 connote the ternary values to represent false, undefined, and true, respectively. Various fields with their unique characteristics and operators are described in MVL logics such as Literal, Galois, Luka Siewicz, Godel, and Kleene (Mukaidono 1986). Each field consists of a number of functions and basic operators.

The first two values of every logical system are obviously "true" and "false". The additional value in Kleene system is "undefined" or "undetermined" which states the situation that either we don't know what the value is or there is no computable value. In other words, when a logical function can't determine its output, the output is considered "undefined" which is the third value in Kleene's logic.

A good example is the Boolean function factorial (n) > 30. We have written the factorial function like the following:

```
double factorial(double n)
{
 if(n==0)
 return 1;
 else
 return n*factorial(n-1);
}
```

Now, if we give the function an input of a positive integer number, it generates an understandable output which determines our Boolean function's output. But what happens if we input a negative number? Obviously, we will encounter an infinite loop which consumes the entire stack and produces an error. This is why we define the third value **"i"** that in this example is produced whenever we input a negative or non-integer number.

Considering the three-valued structure of Kleene's similar systems, in addition to "truth falseness" we should pay attention to another parameter named "knowledge". Based on this, "t" and "f" are on the same level while "i" is located in a lower one. In some cases, we can define some of the undefined values with changes in the structure. Of course, these changes should only cause the value of "i" to become either "t" or "f". The values changes from "t" to "f" or vice versa are not acceptable. In other words, we expect our "t" and "f" to be very close to the classical values and really represent the trueness and falseness. In case the function is working based on probabilities, with the increase of information, there shouldn't be a change in trueness of any defined sentence. The only change can be from an undefined sentence to a defined one. This quality is named "monotonicity". Considering the definition of "i" and "monotonicity" we can design various systems. Based on their performance, these systems fall into three categories of strong, weak and intermediate (Fitting 1991).

In Kleene's strong three-valued systems, Boolean phrases are calculated in parallel and based on decisive values. For example, for value estimation of p ^ q, p and q are calculated simultaneously. This procedure continues until one of the two sentences return a decisive value. In this case, the phrase is evaluated without the value estimation of the second sentence. However, if no decisive value is established and one of the sentences has "i" value, calculation of the phrase will be infinite which means the whole phrase will have a value of "i". Consequently, the evaluation results will be like table 1.

Table1: Kleene's strong three-valued logic

	~	∧			N			→			↔		
		0	1/2	1	0	½	1	0	1/2	1	0	1/2	1
0	1	0	0	0	0	½	1	1	1	1	1	1/2	0
1/2	1/2	0	1/2	1/2	1/2	½	1	1/2	1/2	1	1/2	1/2	1/2
1	0	0	1/2	1	1	1	1	0	1/2	1	0	1/2	1

In the other type, Kleene's weak three-valued system, for calculating the value of a phrase, first, all the sentences are evaluated. Then the value of the whole system can be calculated based on the results. In conclusion, in all operators, if there is just an "i" operand, the result will be "i" too. Consequently, the evaluation results will be like table 2.

Table2: Kleene's weak three-valued logic

	~		∧			N			→			↔	
		0	1/2	1	0	½	1	0	1/2	1	0	1/2	1
0	1	0	1/2	0	0	½	1	1	1/2	0	1	1/2	0
1/2	1/2	1/2	1/2	1/2	1/2	½	1/2	1/2	1/2	1/2	1/2	1/2	1/2
1	0	0	1/2	1	1	½	1	1	1/2	1	0	1/2	1

Kleene's intermediate three-valued system, like the strong system, uses decisive values in order to calculate the output. However, it has one big difference with the strong system; Calculations are not done in parallel but in sequence. Imagine that we want to evaluate p ^ q in this system and the sequence is from left to right. First, p is evaluated. If it has a value of "f" then we can conclude that the whole phrase has a value of "f" without even checking q (even if q has "i" value). Now, suppose it's the other way around; p has a value of "i" and q has "f" value. First, p is evaluated and then without checking q we can conclude that the whole phrase has a value of "i". Therefore, this system doesn't have the commutative property which makes it not so appealing. Consequently, evaluation results for intermediate systems which calculate phrases from left to right will be like table 3.

Table3: Kleene's intermediate three-valued logic

	~	∧			N			→			↔		
		0	1/2	1	0	½	1	0	1/2	1	0	1/2	1
0	1	0	0	0	0	1	1	1	1	1	1	1/2	0
1/2	1/2	1/2	1/2	1/2	1/2	½	1/2	1/2	1/2	1/2	1/2	1/2	1/2
1	0	0	1/2	1	1	½	1	0	1/2	1	0	1/2	1

For all the three systems mentioned above or any other three-valued logical systems, five main operators are analyzed in order to find out how the system works. These five operators are:

~ negation
^ conjunction
∨ disjunction
⟶ implication
↔ bi-conditional

CNTFET Based Kleene's Three-Valued Logic Circuit Design

Recently, Multiple-Valued Logic has entered the Integrated Circuits' world. Using this logic, we can achieve a higher circuit density while performing more complex operations with less interconnection problems. There are two types of Multiple-Valued logic circuits: current-mode and voltage-mode. Current mode can be implemented using CMOS technology while voltage-mode requires transistors with more than one threshold voltage levels. Therefore, Carbon Nanotube transistors are ideal for this purpose. In this section we try to implement basic functions of Kleene's three-valued logic using CNTFETs and analyze their dynamic parameters.

We have used a new method of CNTFET circuit design which lets us omit the resistors in our circuits (LIN 2009). Therefore, we can design higher performance circuits with lower power consumption, which occupy smaller area as well. In the following circuit designs, we need two threshold voltage levels, which are gained by two different diameters of nanotubes. To achieve these two diameters, we need to have

chiralities of (19, 0) and (9, 0). Using these chiralities, we can have threshold voltage levels of 0.289 Volts and 0.559 Volts for N-CNTFETs and the same but negative voltages for P-CNTFETs.

In the following, we present the simulation results of the three types of Kleene's three-valued logic. We have used a VDD of 0.9 Volts in all these circuits.

Strong Kleene

Here we have simulated the four basic functions of Kleene's strong three-valued logic using the new method of CNTFET circuit design. You can find the logical operation of these functions in the table 1.

Figure 4.a shows the implementation of strong Kleene's conjunction using the new method of CNTFET circuit design. Figure 4.b shows the result of the simulations in Synopsis HSPICE with sample inputs (Deng 2007). When either of the input voltages are less than 0.3V, T1 and T2 transistors are turned on or a short circuit will happen between output and ground. Therefore, the output will have a voltage level of 0 Volts. In case both inputs are between 0.3v and 0.6v or both of them are greater than 0.6v, the pull-up network and a part of the pull down network will be connected to the output line simultaneously. Therefore, we will face a voltage division which leads to an output of VDD/2. If one of the inputs is between 0.3v and 0.6v and the other one is greater than 0.6v, the pull-up network will be connected to the output and we will have an output of VDD.

Figure 5.a shows the implementation of strong Kleene disjunction using the new method of CNTFET circuit design. Figure 5.b shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, if both inputs are less than 0.3V, the pull-down network will be connected to the output and causes an output of 0 Volts. When one of the inputs is between 0.3V and 0.6V and the other one is less than 0.6V, the pull-up network and a part of the pull-down network will be connected to the output. Therefore we will face a voltage division which leads to an output of VDD/2. Finally, when either of the inputs is more than 0.6V, the pull-up network will be connected to the output and we will have an output voltage of VDD.

Figure 6.a shows the implementation of strong Kleene implication using the new method of CNTFET circuit design. Figure 6.b shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, if the first input (a) is more than 0.6V or the second input (b) is less than 0.3V, the pull-up network will be connected to the output and the result will be VDD. In this circuit, there are two situations when the pull-up network and a part of the pull-down network are connected to the output simultaneously and cause an output of VDD/2: 1-When "b" is between 0.3V and 0.6V and "a" is less than 0.6V. 2-When "a" is between 0.3V and 0.6V and "b" is greater than 0.6V. Finally, when "b" is greater than 0.6V and "a" is less than 0.3V, pull-down network will be connected and an output of 0 Volts will be generated.

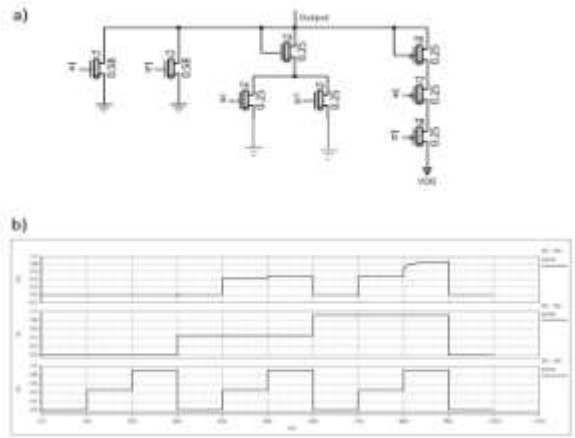

Figure 4: a) Strong Kleene conjunction circuit design; b) Simulation results

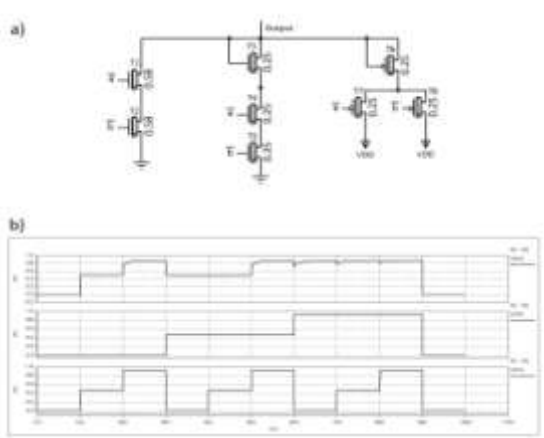

Figure 5: a) Strong Kleene disjunction circuit design; b) Simulation results

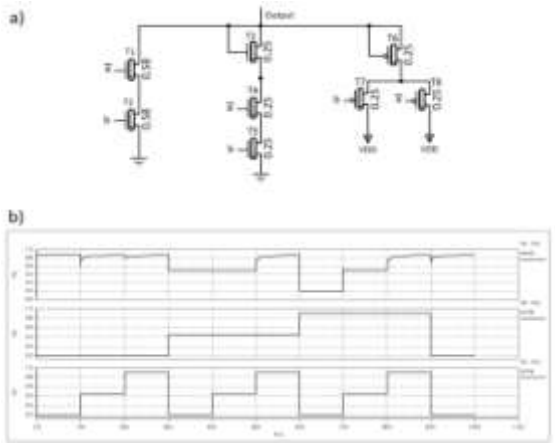

Figure 6: a) Strong Kleene implication circuit design; b) Simulation results

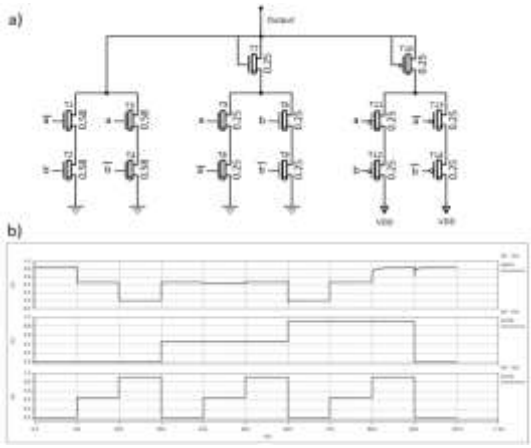

Figure 7: a) Strong Kleene bi-conditional circuit design; b) Simulation results

Figure 7.a shows the implementation of strong Kleene bi-conditional function using the new method of CNTFET circuit design. Figure 7.b shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, in case one input is less than 0.3V and the other one is greater than 0.6V, pull-down network will be connected to output line and an output of 0 Volts will be generated. If either of the inputs is between 0.3V and 0.6V,the pull-up network and a part of the pull-down network are simultaneously connected to the output line. Due to voltage division that happens, we will face an output of VDD/2. Finally, if both inputs are less than 0.3V or more than 0.6V, the pull-up network will be connected to the output line and VDD will be generated as the function's output.

Week Kleene

Here we have simulated the four basic functions of Kleene's weak three-valued logic using the new method of CNTFET circuit design. You can find the logical operation of these functions in the table 2.

Figure 8.a shows the implementation of weak Kleene conjunction using the new method of CNTFET circuit design. Figure 8.b shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, there are two sets of input voltage levels which can cause the pull-down network to connect to the output line and generate 0V output: 1-When both inputs are less than 0.3V. 2-When one input is less than 0.3V and the other one is greater than 0.6V. On the other hand, if either of the inputs is between 0.3V and 0.6V, the pull-up network and a part of the pull-down network will be connected to the output line simultaneously which can cause an output of VDD/2 due to the voltage division that happens. Finally, when both inputs are greater than 0.6V, the pull-up network will be connected to the output line and an output of VDD will be generated.

Figure 9.a shows the implementation of the weak Kleene disjunction using the new method of CNTFET circuit design. Figure 9.b shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, when both inputs are less than 0.3V the pull-down network will be connected to the output line and we will face an output of 0 Volts. On the other hand, if either of these inputs is between 0.3V and 0.6V, the pull-up network and a part of the pull-down network will be connected to the output line simultaneously. Therefore, a voltage division will happen which generates an output of VDD/2. Finally, if both inputs are greater than 0.6V or one is less than 0.3V and the other one is greater than 0.6V, the pull-up network will be connected to the output line which will generate an output of VDD.

Figure 10.a shows the implementation of weak Kleene implication using the new method of CNTFET circuit design. Figure 10.b shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, when the first input (a) is greater than 0.6V and the second input (b) is less than 0.3V, an output of 0 Volts will be generated. On the other hand, if either of the inputs is between 0.3V and 0.6V, the pull-up network and a part of the pull-down network will be connected to the output line simultaneously. Therefore, we a voltage division will happen which leads to an output of VDD/2. There

are two situations which lead to an output of VDD: 1-When both inputs are less than 0.3V. 2-When "a" is less than 0.3V and "b" is greater than 0.6V.

Circuit design and simulation results for weak Kleene bi-conditional function are exactly the same as the ones for strong Kleene. Hence, there is no need to present them here again.

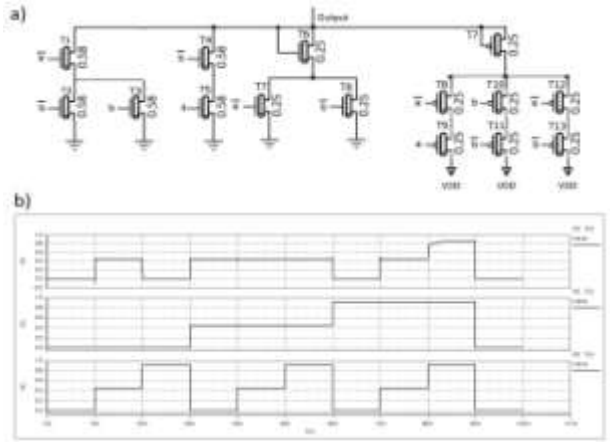

Figure 8: a) Weak kleene conjuction circuit design; b) Simulation results

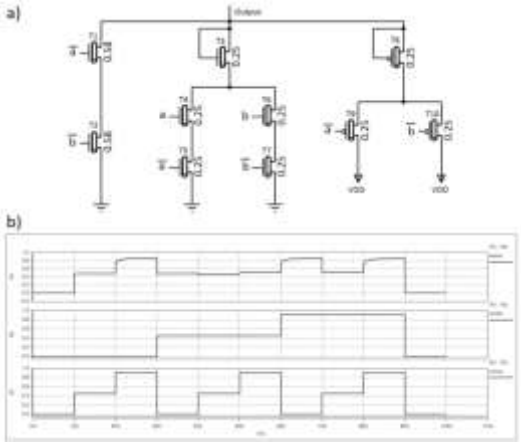

Figure 9: a) Weak kleene disjuction circuit design; b) Simulation results

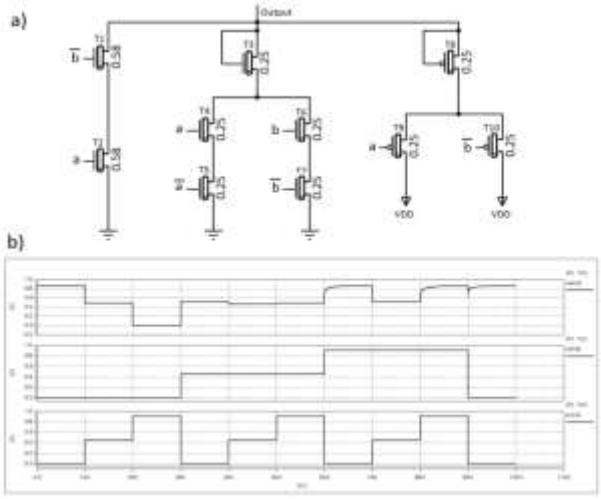

Figure 10: a) Weak kleene implication circuit design; b) Simulation results

Intermediate Kleene

Here we have simulated the four basic functions of Kleene's intermediate three-valued logic using the new method of CNTFET circuit design. You can find the logical operation of these functions in the table3. Figure 11.a shows the implementation of intermediate Kleene conjunction using the new method of CNTFET circuit design. Figure 11.b shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, there are two situations that lead to an output of 0 Volts: 1-When the second input (b) is less than 0.3V. 2-When the first input (a) is less than 0.3V and "b" is greater than 0.6V. There are two other situations which cause the pull-up network and a part of the pull-down network to be connected to the output line simultaneously and generate an output of VDD/2 due to the voltage division that occurs: 1-When "b" is between 0.3V and 0.6V. 2-When "a" is between 0.3V and 0.6V and "b" is greater than 0.3V. Finally, if either of the inputs are greater than 0.6V, an output of VDD will be generated.

Figure 12.a shows the implementation of the intermediate Kleene disjunction using the new method of CNTFET circuit design. Figure 12.a shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, when either of the inputs is less than 0.3V an output of 0 Volts is generated. On the other hand, if the second input (b) is between 0.3V and 0.6V or the first input (a) is between 0.3V and 0.6V and a is greater than 0.3V, the pull-up network and a part of the pull-down network will be connected to the output line simultaneously. Therefore, we will face an output of VDD/2. There are three situations which an output of VDD is produced as a result: 1-When one input is less than 0.3V and the other one is greater than 0.6V. 2-When "a" is between 0.3V and 0.6V and "b" is less than 0.3V. 3-When either of the inputs is greater than 0.6V.

Figure 13.a shows the implementation of intermediate Kleene implication using the new method of CNTFET circuit design. Figure 13.b shows the result of the simulations in Synopsis HSPICE with sample inputs. In this circuit, when the first input (a) is less than 0.3V and the second one (b) is greater than 0.6, an output of 0 Volts will be generated. On the other hand, if "b" is between 0.3V and 0.6V or "a" is between 0.3V and 0.6V and "b" is greater than 0.3V, pull-up network and a part of pull-down network will be connected to the output line which results in an output of VDD/2. Finally, if "b" is less than 0.3V or either of the inputs is greater than 0.6V, an output of VDD will be generated.

Circuit design and simulation results for intermediate Kleene bi-conditional function are exactly the same as the ones for strong Kleene. Hence, there is no need to present them here again.

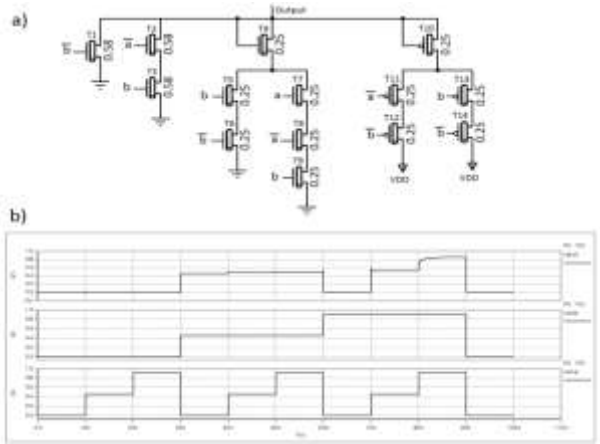

Figure 11: a) Intermidiate kleene conjuction circuit design; b) Simulation results

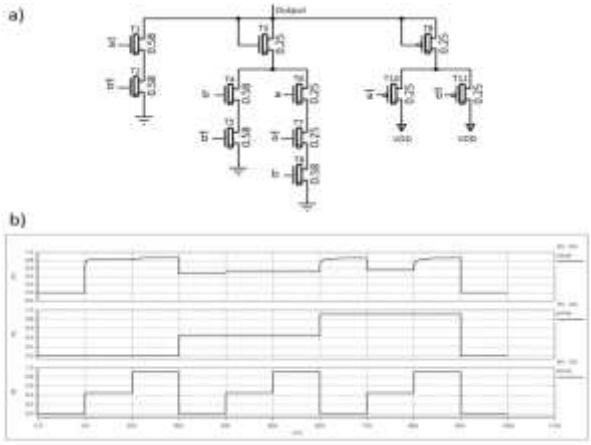

Figure 12: a) Intermidiate kleene disjuction circuit design; b) Simulation results

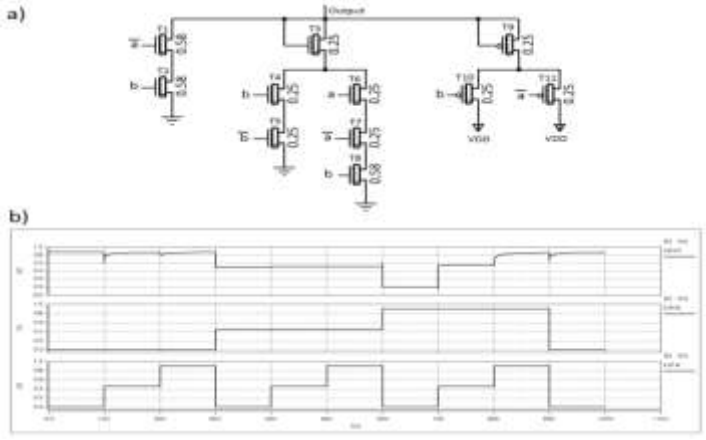

Figure 13: a) Intermidiate kleene implication circuit design; b) Simulation results

Experimental Results and Optimization of Dynamic Parameters

In this section, the proposed designs are simulated at different supply voltages and temperatures using Synopsys HSPICE. In all situations we measured the average propagation delay and power consumption. In order to make the trade-off between delay and average power consumption parameters, the PDP metric is calculated, which is the average delay multiplied by average power consumption. In the first experiment, the circuits are simulated at 0.9V and 1V supply voltages; and in the second one, the circuits are simulated at 7°C, 27°C, 47°C and 67°C temperatures.

When the voltage of power supply increases, the simulation results show that the propagation delay will be decreased while power consumption increases. The effects of voltage changes on propagation delay, power consumption and PDP are depicted respectively in table.4, table.5 and table.6.Reducing the supply voltage decreases the power consumption, but it increases propagation delay. It was found that for the best performance, the supply voltage must be set around 0.9 V.

Table 4: Variation of delay with different supply voltage for kleene logic

	Vdd(V)	
Delay(* 10 $^{-12}$s)	0.9	1
Strong Kleene conjunction	6.4625	4.0391
Strong Kleene disjunction	6.8908	5.2123
Strong Kleene implication	10.4052	7.8024
Strong Kleene bi-conditional	11.3549	7.0268
Weak Kleene conjunction	11.7052	5.9541
Weak Kleene disjunction	12.7361	10.5367
Weak Kleene implication	16.7264	6.7373
Intermediate Kleene conjunction	6.0331	4.2032
Intermediate Kleene disjunction	13.2189	13.4898
Intermediate Kleene implication	6.4073	6.8862

Table 5: Variation of power with different supply voltage for kleene logic

	Vdd(V)	
Power(* 10 $^{-7}$ W)	0.9	1
Strong Kleene conjunction	1.1325	1.9885
Strong Kleene disjunction	0.1948	0.2735
Strong Kleene implication	2.0721	3.0478
Strong Kleene bi-conditional	1.7870	2.8261
Weak Kleene conjunction	0.6481	1.1482
Weak Kleene disjunction	0.6638	0.9832
Weak Kleene implication	0.6662	0.9839
Intermediate Kleene conjunction	0.3540	0.6184
Intermediate Kleene disjunction	0.4382	0.6269
Intermediate Kleene implication	0.5827	0.8915

Table 6: Variation of PDP with different supply voltage for kleene logic

	Vdd(V)	
PDP(* 10 $^{-19}$J)	0.9	1
Strong Kleene conjunction	7.3187	8.0317
Strong Kleene disjunction	1.3416	1.4255
Strong Kleene implication	21.5606	23.7801
Strong Kleene bi-conditional	20.2912	19.8584
Weak Kleene conjunction	7.5861	6.8364
Weak Kleene disjunction	8.4542	10.3596
Weak Kleene implication	11.1431	6.6288
Intermediate Kleene conjunction	2.1357	2.5992
Intermediate Kleene disjunction	5.7925	8.4567
Intermediate Kleene implication	3.7335	6.1390

The simulation results in different temperatures demonstrate that the proposed designs have an appropriate performance and regular functionality in a massive range of temperatures (figure 14, figure 15 and figure 16).

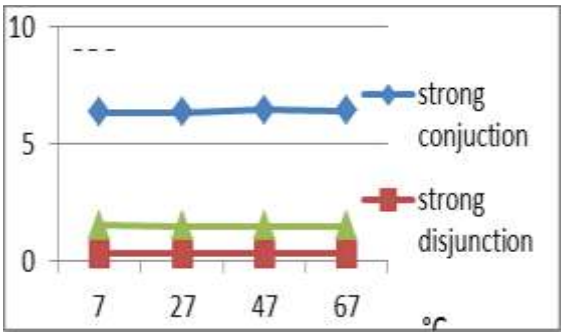

Figure 14: Variation of PDP with different temperatures for strong Kleene

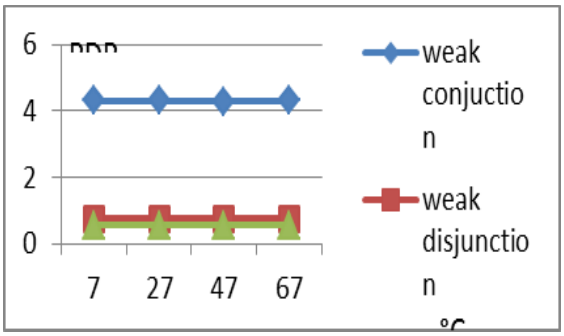

Figure 15: Variation of PDP with different temperatures for weak Kleene

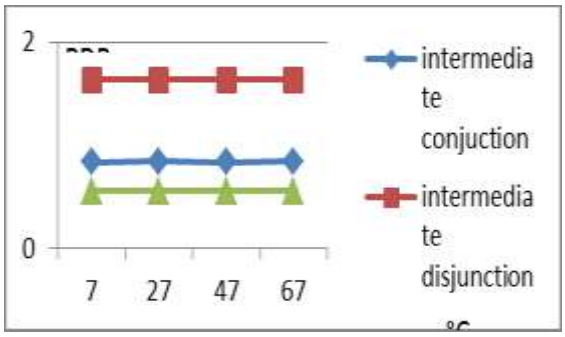

Figure 16: Variation of PDP with different temperatures for intermediate Kleene

CONCLUSION

In this paper, we have presented a novel circuit design technique to implement Kleene's three-valued logic by using carbon nanotube field effect transistors. We have achieved a significant improvement in delay, power and power-delay product. Based on Kleene's family performance, these systems fall into three categories of strong, weak and intermediate. We have simulated the four basic functions of Kleene's strong, Kleene's weak and Kleene's intermediate three-valued logic using the new method of CNTFET circuit design. Simulation results using Synopsis HSPICE show the accuracy of our optimizations.

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