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Research Article

DESIGNING A NEW RING OSCILLATOR FOR HIGH PERFORMANCE APPLICATIONS IN 65nm CMOS TECHNOLOGY

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ABSTRACT
In this paper, a novel seven-stage ring oscillator with optimized power consumption and phase noise functionality, suitable for high frequency applications in phase-locked loops is designed and implemented. An innovative new cell with optimized structure is used to design the ring oscillator. The proposed circuit has been implemented using a differential Gilbert cell structure. In addition, the researchers have used different techniques including proper sizing of transistors and PMOS transistor as an active load and a new structure is presented to reduce delay and die area. As a result, the amount of power consumption of the ring oscillator has been optimized. Furthermore, circuit performance and figure of merit have been increased to a large extent. The ring oscillator is simulated through using 65nm CMOS technology and in the central frequency of 25GHz has -137.6 dBc/Hz phase noise, 2.49mW power consumption and -221.6 dBc/Hz figure of merit. H-Spice and Mat lab software were used to simulate and analysis the ring oscillator.

Keywords: *Phase-Locked Loop, Voltage Controlled Oscillator, Ring Oscillator, Phase Noise*

INTRODUCTION
In recent years, the use of high-frequency integrated circuits for wireless telecommunications has gained attention. Voltage controlled oscillator is considered as building blocks of analog and digital circuits and plays a vital role in phase-locked loops. Voltage controlled oscillator is used in a variety of electronic systems such as frequency synthesizer, phase-locked loops, telecommunications systems, receivers and transmitters. Phase-locked loop is a key element in many high-speed systems and provides schedule basis for functions such as clock control, data recovery, and synchronization (Stauth and Liang, 2003; Eken and Uyemura, 2004). Synchronization requires a phase-locked loop for implementation. For high performance applications a designed voltage controlled oscillator requires high-speed, low phase noise, and negligible power consumption. It also should occupy extremely small surface on a chip.

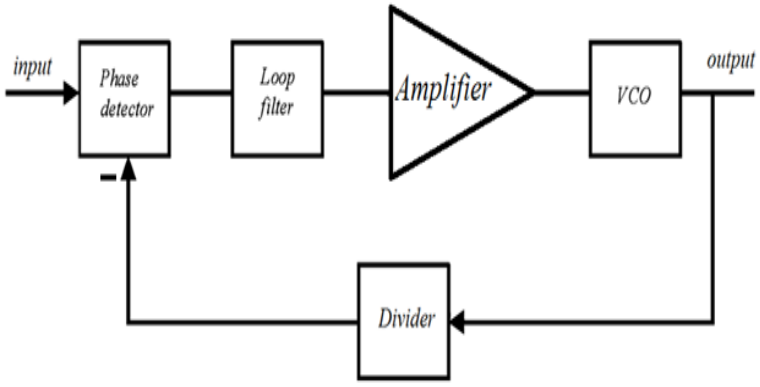

Figure 1: PLL Block diagram and its components

Voltage controlled oscillators can be LC oscillator or ring oscillator. One of the disadvantages of LC oscillators is that they occupy a large chip area due to using an inductor in their structure. However, LC oscillators have better noise phase performance than ring oscillators. Thus, nowadays, ring oscillators are

put to use due to occupying minimal area on chip. Ring oscillators have wide tuning range in comparison with LC oscillators.

Various techniques are used to amend and improve the performance of the ring oscillator such as transistor sizing. PLL Block diagram is shown in figure 1. According to figure 1, a PLL consists of components such as phase detector, filter, amplifier, voltage controlled oscillator and frequency divider. In this paper, differential topology has been used for the voltage controlled oscillator. The oscillator consists of seven-stage voltage controlled ring oscillator, and benefits from high-speed, low power consumption, and low phase noise.

Barkhausen principle is used for designing ring oscillators. According to Barkhausen principle, first criterion for oscillation in oscillators is an appropriate phase shifts of 180° so that each stage has $\frac{180^{\circ}}{N}$ contribution to phase shift. Second criterion for oscillation is that the loop gain should be greater than 1 (Razavi, 2000), (Finnstam and Soderlund, 2005). For the ring oscillator to be able to oscillate at least three stages are required (Razavi, 2000), (Finnstam and Soderlund, 2005). There are several factors that affect the performance of ring oscillator such as power consumption, phase noise, noise, supply voltage, distortion, oscillation frequency, etc., and there need to be a tradeoff between one parameter and the other parameters. These parameters should be considered in the optimization. Accurate calculation of the oscillation frequency is also one of the important factors in designing oscillators.

The Structure of a Voltage Controlled Ring Oscillator

Differential voltage controlled ring oscillator is capable of adjusting gain in the supply voltage. The output voltage swing of the oscillator depends on its supply voltage. In differential topology, the common mode eliminates noise and causes the output to be safe against the noise. Other advantages of utilizing differential topology include being easy to control delay in delay cells, being capable of using odd or even number of delay cells, and having high security against power supply disruptions (Kumar and Kaur, 2012).

In order to have a high-frequency oscillator the delay in delay cell should be reduced as much as possible. By reducing power consumption, increasing phase noise efficiency, and increasing the tuning range we can have a high performance ring oscillator at high frequencies. Block diagram of a n stage voltage controlled ring oscillator is shown through differential topology in figure (2). The stages are coupled together in a cascade fashion and output of last stage is connected in reverse to input of first stage through using a feedback loop. Delay cell are completely identical in these stages.

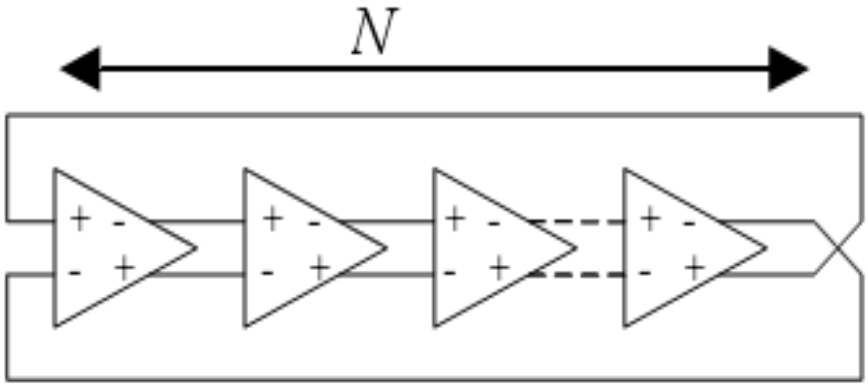

Figure 2: N stage ring oscillator with differential structure

Various architectures have been proposed by researchers for a voltage controlled oscillator. Delay cell (Eken and Uyemura, 2004) has a good tuning range; however, its phase noise performance and power consumption are not acceptable. Oscillator designed in (Jalil *et al.*, 2012) has an acceptable frequency; however, its tuning range is narrow. Although the proposed circuit (Kim *et al.*, 2013) benefits from a good phase noise, its frequency is not considerable. In this paper, we try to make a good compromise

between phase noise and other parameters influencing oscillator performance. The frequency at which ring oscillator oscillate is calculated through equation (1).

(1) $f_{osc} = \frac{1}{2.N.t_d}$

In this equation N is the number of individual inverter stage. According to the above equation, to increase frequency, stages should be few in number and t_d should be negligible. In this case, oscillator frequency increases.

The Proposed Voltage Controlled Oscillator

In this paper a seven stage voltage controlled ring oscillator with differential topology is proposed for high frequencies. The proposed delay cell for this ring oscillator is shown in figure 3. In this figure, M_C converts bias voltage into a current. In fact, the transistor is a current source. This current is equal to the sum of the current source transistors M1-M4. In most CMOS technologies fabricating resistances with the exact value, and sensible physical sizes is difficult. If in a MOSFET transistor, gate and drain are shorted together, it can function as a two terminal resistance in small signal model. This combination is called a diode device. In figure (3), M5 and M6 are diode devices and function as a resistance.

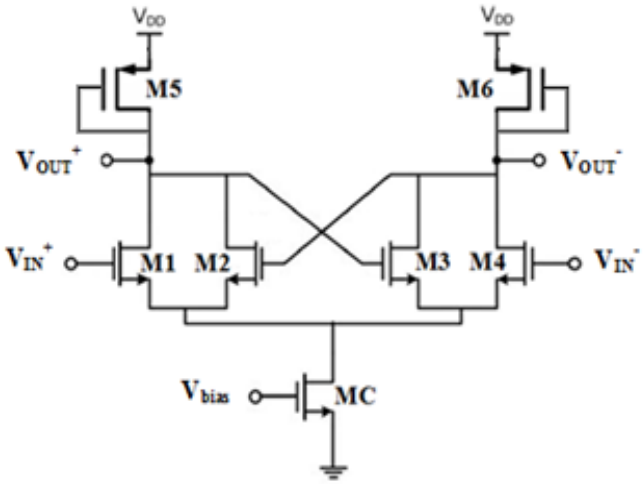

Figure 3: Delay Cell

Simulation of a Ring Oscillator

Simulation of oscillator circuit has been done using H-Spice software. The waveform of differential outputs of delay cell for supply voltage of 1.1 volts is shown in figure (4). In this mode, the delay cell frequency is 25GHz.

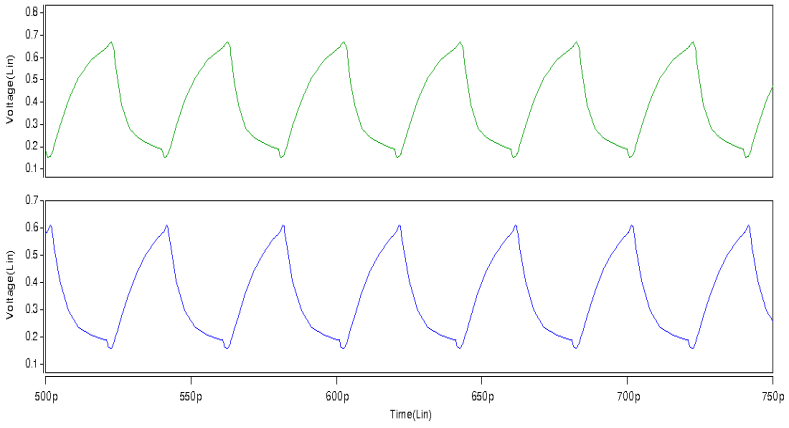

Figure 4: The output waveform of delay cell

The proposed ring oscillator has been simulated at high frequency using 65nm technology. The output waveform obtained from the seven stage ring oscillator simulation is shown in figure (5) using H-spice software. The oscillator frequency is 25GHz. The results of proposed ring oscillator simulation can be seen in table 1.

Table 1: The results of the proposed ring oscillator simulation

Number	V_{dd}	V_{bias}	F_{osc}	Power Consumption
1	1	1	15.87GHz	1.49mW
2	1.2	1	19.80GHz	2.44mW
3	1.3	1	23GHz	2.96mW

In the above table the rate of oscillation frequency was different for variable values of the power supply and constant values of the other parameters. It can be seen that the oscillator frequency increases with increasing supply voltage. The oscillation frequency of 23GHz was obtained for 1.3 V supply voltage.

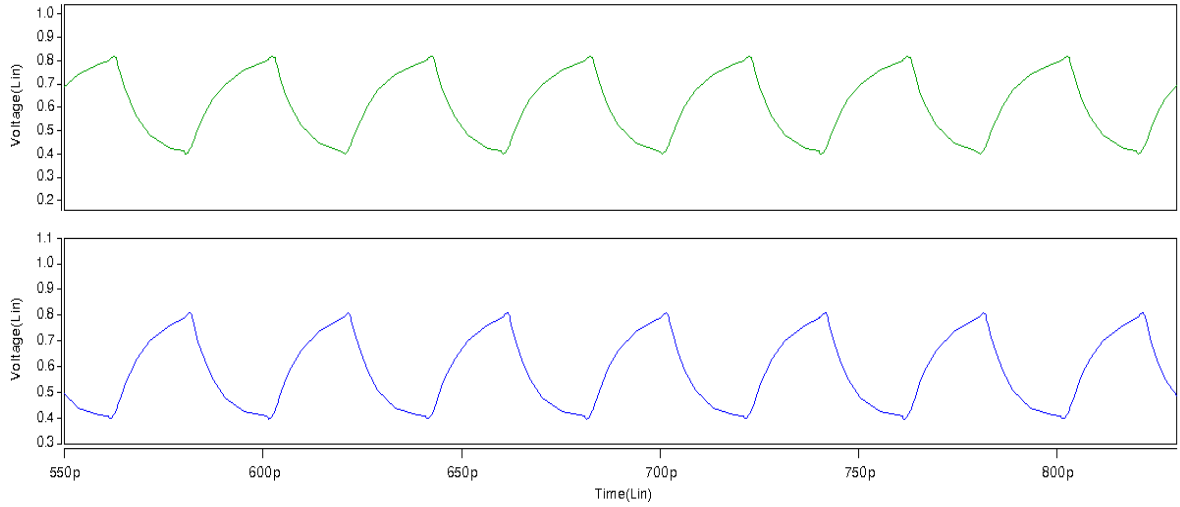

Figure 5: Frequency waveform of a ring oscillator at a frequency of 25 GHz

Phase Noise

Phase noise is a feature of true signals that occurs as a result of a small and uncertain random change in signal phase. Phase noise creates a fundamental limitation on system performance and limiting the dynamic range. Thermal noise of transistors and Flicker noise are considered as factors intensifying the phase noise. Figure 6 shows the different areas of noise phase. Area $1/f^2$ due to thermal noise and area $1/f^3$ due to low frequency noise are considered as Flicker noise in MOS devices. Phase noise in areas $1/f^2$ and $1/f^3$ is calculated by the equation (2) and (3) respectively.

$$(2)\ L(d\omega) = 10\log\left(\frac{\Gamma^2_{rms}}{q^2_{max}}.\frac{\bar{i}^2_n/\Delta f}{2d\omega^2}.N\right)$$

$$(3)\ L(d\omega) = 10\log\left(\frac{\Gamma^2_{dc}}{q^2_{max}}.\frac{\bar{i}^2_n/\Delta f}{2d\omega^2}.\frac{\omega_{1/f}}{df}.N\right)$$

N is total number of stages of ring oscillator, $\bar{i}^2_n/\Delta f$as and $\omega_{1/f}$ are current spectral density due to thermal noise and flicker noise of components, and q_{max} is maximum load at the output node. According to

equations (2) and (3), phase noise is directly correlated to thermal noise and flicker noise. Reducing thermal noise and flicker noise can cause phase noise to decline significantly. The less number of stages may also cause phase noise to be reduced. On the other hand, the smaller the size of transistors, to the same extent the smaller their thermal noise and flicker noise become.

In this paper it has been tried to reduce sizing of transistors to the least amount possible. Such an action not only can cause oscillator power consumption to be reduced, but also it is effective in reducing thermal noise. Finally, oscillator phase noise can also be reduced through using this method. The value of proposed ring oscillator phase noise is -137.6dbc/Hz at 1Hz offset. The phase noise waveform at 25GHz center frequency is shown in figure (7). The value of figure of merit is equal to -221.6dBc/Hz at 25GHz frequency.

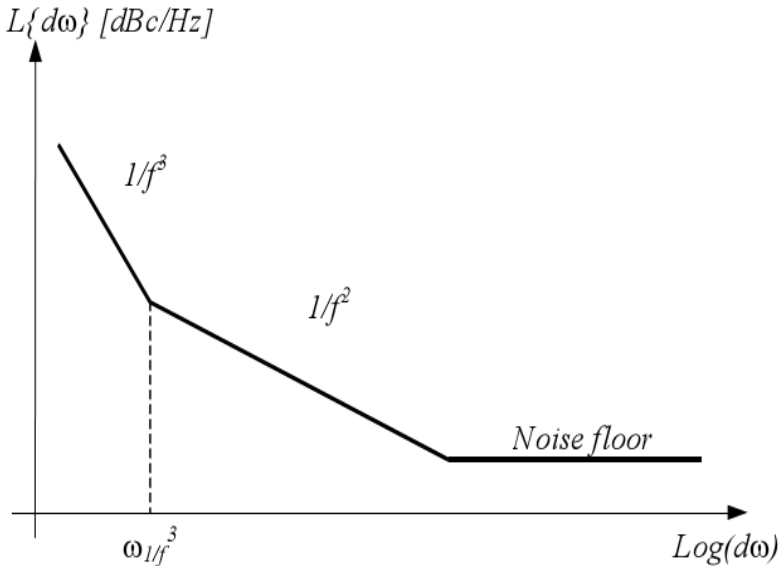

Figure 6: Different regions of phase noise

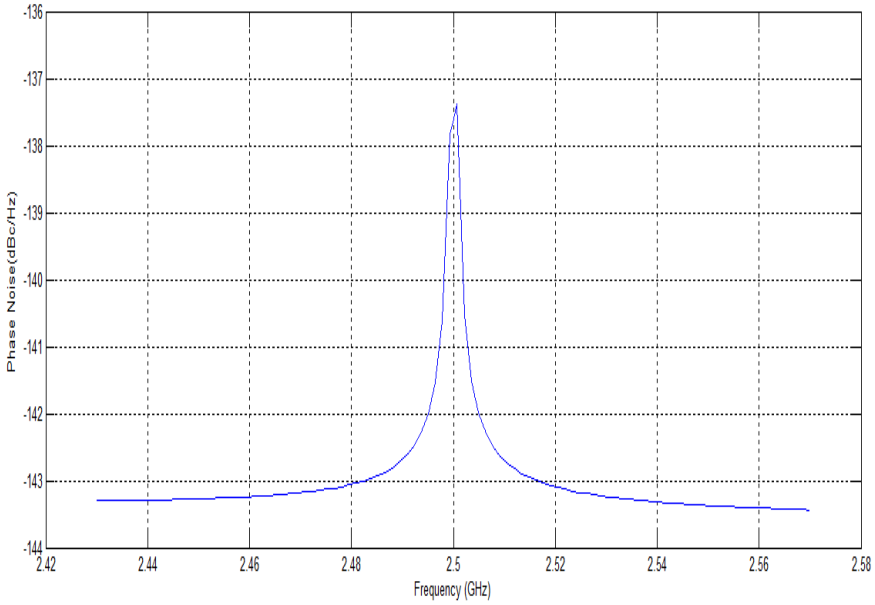

Figure 7: Phase noise at 25GHz center frequency

Table 2: Comparison between articles

References	Raman *et al.*, (2012)	Ramiah *et al.*, (2012)	Joo-Myoung *et al.*, (2013)	Vandna *et al.*, (2013)	In this work
Power Supply	1.8V	1.8V	1V	0.7V	1.2V
Voltage of Control	1V- 1.8V	0.6V – 1V	---	---	---
Power Consumption	0.621mW	1.09mW	10mW	1.92µW	2.49mW
Frequency		2.4GHz	465MHz	341MHz	25GHz
Phase Noise	---	-141dBc/Hz at 1-MHz offset	-110.8dBc/Hz at 1-MHz offset	0.34kdBc/Hz	-137.6dBc/Hz at 1-MHz offset
FOM	---	-208.23dBc/Hz	-157dBc/Hz	---	-221.6dBc/Hz
Technology	0.18µm	0.18µm	65nm	45nm	65nm
Number of stage	3	3	4	9	7
Year	2012	2012	2013	2013	2014

A comparison between the previous studies and the present study can be found in Table 2. It can be observed in the table that the designed oscillator has been optimized regarding parameters such as oscillation frequency, phase noise and figure of merit compared to previous research. In addition, the amount of supply voltage required is reduced.

CONCLUSION

The present study indicates a 25GHz ring oscillator with high performance and minimal phase noise. The proposed ring oscillator is one of the important components of phase-locked loop. The simulation of this oscillator has been done by H-spice software using 65nm technology. We were able to optimize the proposed oscillator phase noise through reducing noise sources which included thermal noise and flicker noise. At 25GHz frequency, the value of phase noise is -137.6dbc/Hz at 1MHz offset. The figure of merit of the proposed ring oscillator is -221.6dBc/Hz. The proposed ring oscillator can be used for high-speed applications requiring low noise and minimal power supply.

REFERENCES

Eken YA and Uyemura JP (2004). A 5.9-GHz Voltage-controlled Ring Oscillator in 0.18-µm CMOS, *IEEE Journal of Solid-State Circuits* **39(**1) 230-233.

Finnstam P and Soderlund M (2005). Design of CMOS ring oscillator, circuit Design Group Department Of signals and systems chalmers University of Technology Goteborg, Sweden.

Joo-Myoung Kim, Seungjin Kim, In-Young Lee, Seok-kyun Han and Sang-Gug Lee (2013). A Low Noise Four-Stage Voltage Controlled Ring Oscillator in Deep-Submicrometer CMOS Technology. *IEEE Transactions on Circuits and System-II* **60**(2).

Jubayer Jalil, Manum Bin Ibne Reaz, Labonnah Farzana Rahman, Mohammad Marufuzzaman and Mohammad Syedul Amin (2012). A 2.45 GHz CMOS Voltage Controlled Ring Oscillator for Active Transponder, The Fifth International Conference on Advances in Circuits, Micro-electronics.

Kumar S and Kaur G (2012). Design and Performance Analysis of Nine stages CMOS based Ring Oscillator, *International Journal of VLSI Design & Communication Systems* (VLSICS) **3**(3).

Raman A, Nidhivashishtha J and Sarin RK (2012). London, U.K A RF Low Power 0.18µm based CMOS Differential Ring Oscillator, *Proceedings of the World Congress on Engineering* **2**.

Ramiah H, Keat CW and Kanesan J (2012). Design of Low-phase, Low-power Ring Oscillator for OC-48 Application. *IETE Journal of Research* **58**(5).

Razavi B (2000). *Design of Analog CMOS Integrated Circuits* (McGraw-Hill series in Electrical and Computer and Engineering, Boston).

Tauth J and Liang A (2003). Jitter Optimization Using the Body Bias in Digital CMOS Ring Oscillators, U.C. Berkeley.

Vandna Sikarwar, Neha Yadav and Shyam Akashe (2013). Design and Analysis of CMOS ring oscillator using 45nm technology. *IEEE Advance Computing Conference*.