

**Research Article**

## REPRESENTING A NEW ADDER IN ONE-HOT RESIDUE NUMBER SYSTEM

\*Morteza Fathi<sup>1</sup>, Sara Ebrahimi<sup>1</sup> and Kooroush Manouchehry<sup>2</sup>

<sup>1</sup>Department of Computer Engineering, Amirkabir University of Technology, Tehran, Iran

<sup>2</sup>Parand Branch, Islamic Azad University, Parand, Iran

\*Author for Correspondence

### ABSTRACT

In many arithmetic circuits such as adders, the flow of carry bit from the least significant bit to the most, causes reducing speed and the performance of the circuit. Residue Number System (RNS) is an appropriate system for fast and parallel arithmetic operation. This speed increases if One-Hot Residue (OHR) number system is used. There are problems in OHR with area and hardware consumption, when modules are large or result of various arithmetic operation is needed. The problem of carry bit is solved in OHRNS to some extent. There are two concerns related to the application of this Number System: reaching the most possible speed and the largest dynamic range. There is a conflict when one wants to resolve both these problem. That is augmenting the dynamic range results in reducing the speed in the same time. In this paper a novel design of one-hot adder is represented for reducing hardware consumption and the size of circuit. This circuit is useable for Multiple Valued Logic module, in comparison to other RNS design; this circuit has considerably improved the number of transistors and power consumption.

**Keywords:** Residue Number System (RNS), One-Hot, Computer Arithmetic

### INTRODUCTION

RNS has a great potential in Digital Signal Processing, Fast Fourier Transform (FFT), Ad-Hoc Networks and other applications. If one-hot residue number system (OHR) be used in arithmetic operations, it increases the speed of residue number system. If the selected module is  $m$ , then the amount of hardware in modular add or subtract in OHR using barrel shifter is in the order of  $m^2$ . This rate will cause problem when two or more barrel shifters are needed in the circuit. For example when we need both add and subtract operations then we have two barrel shifters. In this case amount of hardware is equal to  $2m^2$  (Ramirez *et al.*, 2002); (Somayeh and Keivan, 2009). Labafniya *et al.*, (2010), has proposed new circuits for one hot residue addition and subtraction using one barrel shifter structure. The proposed circuits have reduced amount of hardware and are able to generate the addition and subtraction results simultaneously (Labafniya and Eshghi 2010).

In Farshidi *et al.*, (2010), new adders for modulo  $(r^n-1)$  with improvements power consumption are proposed. The authors have reached a significant reduction of applied transistors by scarifying the speed of the circuit and increasing the delay in comparison with the conventional OHR adders (Farshidi *et al.*, 2010).

The rest of paper is organized as follows. In section 2, a background of one hot residue number and one hot is presented. In section 3 the proposed one hot add and subtract design in OHRNS system is represented. We introduce a new adder in OHRNS in Section4, Comparison between this proposed design and usual adder is shown in section 5. Section 6 is conclusion of the paper.

### Residue Number System

Residue Numbers System is a non-weight number system and one of its properties is limited distribution of carry numbers between modules in calculations. This system performs calculations on residue numbers simultaneously instead of a large number that considerably increases calculation speed and decreases power consumption. Residue Numbers System is used more in operators with repeated addition, subtraction and multiplies operations. Some of these applications include Digital Signals Processing, Digital Image Processing, Digital Filtering and etc. Application of this system causes increasing of

**Research Article**

calculation speed, decreasing of hardware circuit complexity and chip area and also good implementation of VLSI circuits.

Residue Numbers System based on module sets is defined as  $m_i, i = 1, 2 \dots n$  which relatively prime numbers, that is:

$$\text{GCD}(m_i, m_j) = 1, \quad i \neq j \tag{1}$$

And decimal value of  $x$  in non-weight system of residue numbers is shown as following:

$$\begin{aligned} x &= (x_1, x_2, \dots, x_n) & x_1 &= X \bmod m_i \\ \exists q \rightarrow X &= q_i \cdot m_i + x_i & \text{where } i &= 1, 2, \dots, N \end{aligned} \tag{2}$$

Where,  $x_i$  obtains from remainder of division  $X$  by  $m_i$ .  $M = \prod_{i=1}^n m_i$  is dynamic range of this number in this system and  $x$  can be shown in this system as  $X = (x_1, x_2, \dots, x_n)$  with the original form of that is a unique value for each integer and also  $\alpha$  in  $X \in [\alpha, M + \alpha)$  is a unique integer number (Taleshmekaeil and Mousavi, 2010).

Calculation operation in Residue Numbers System classified in simple and difficult operations groups. Addition, subtraction and multiply are among simple operation group while sign detection and value comparison are among difficult operation group (Hosseinzadeh et al., 2007).

**One-Hot Residue Number System (Ohrns)**

One method of increasing the speed in the arithmetic operation, using the One-hot coding. We use for their presentation number in the module  $m_i$  of the  $m$  signals in the system when any moment only one signal is active and the rest of the signal is disabled and any active signals that indicate the remaining in the corresponding is module.

For the representation value number in this system, module remaining is from zero to  $m_i - 1$ . Residue Numeral System circuit's implementation with One-hot having a regular structure are simple. Implementation of addition circuits remaining by the One-hot is done in rotating shifts (Hosseinzadeh et al., 2007).

Representation number of decimal, binary and one hot residue module  $m_i$  is shown in Table 1.

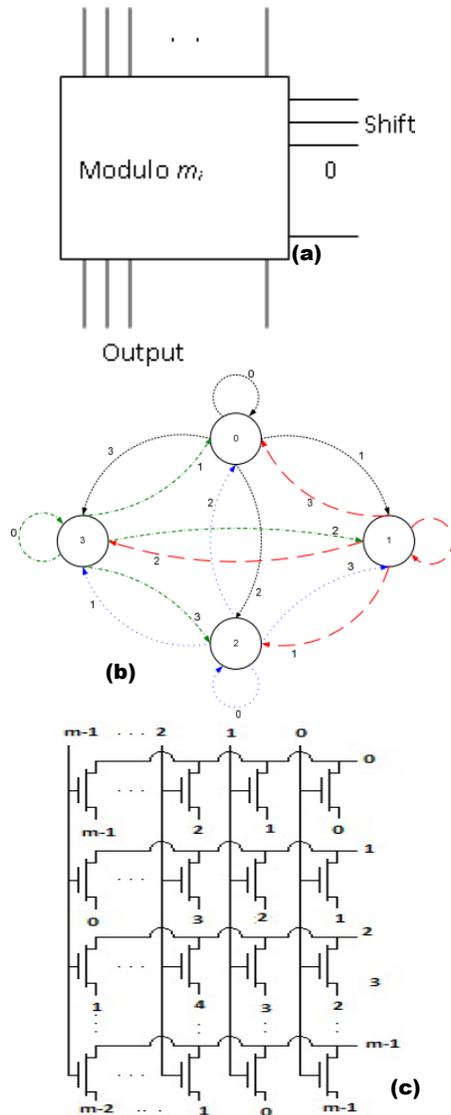
**Table 1: Decimal binary and one hot residue module  $m_i$**

Decimal	Binary	One-hot
0	000...00	1000...0
1	000...01	1000...0
2	000...10	0010...0
.	.	.
.	.	.
.	.	.
$m^i - 1$	000...01	0000...1

One-hot addition structure for  $m_i$  module:

The input data structure (first data) as input value (second data) is shifted and the output is shown. This delay circuit is the size of a transistor Figure 1.

**Research Article**



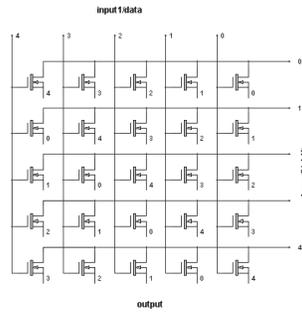
**Figure 1: a) Block diagram of the one hot adder b) Addition position for module four c) Internal structure of the One-hot adder circuit for a module of  $m_i$**

To operation addition such as the subtraction operation is just the input data (first data) the size of the shift value (data second) shift will be reverse (Farshidi *et al.*, 2010).

Of problems in implementation this type of circuit with a One-hot for implement large module because the number of transistors in this structure rises to power. So for large module are not recommended. In order to module set  $\{2n-1, 2n, 2n+1\}$  by putting value  $n = 2$  to module set of  $\{3, 4, 5\}$  that reached to implement this system is appropriate.

Delay of this circuit is equal the delay of only one transistor. However, the amount of needed hardware is in the order of  $m_i^2$ , where  $m_i$  is selected module. For example in figure 3, an adder for module 5 ( $m=5$ ) is presented. Delay of this adder is equal to delay of one transistor. 25 transistors are needed to compose this circuit. Subtract circuit is similar to add circuit with two differences. In the adder, data input is shifted to right, but in the subtractor it is shifted to the left. Another difference is order of input-2 to the circuit. This order is reverse in subtractor, compare to the adder. In figure 4, circuit of a subtractor for module 5 is shown. The output of subtracted has one bit shift in compare to the adder. Both of add and subtract circuits have symmetric shape.

**Research Article**



**Figure 2: One hot adder for module 5**

**The Proposed Adder**

In this section we represent a new method for adding in  $r^n$  module based on One-hot. A is used as the residue in  $r^n$  module that has a range between 0 and  $r^n$ , so we have a N-bit adder that N is equal to the number of A's digits. Then N is divided to 4 parts as shown below:

If N is divisible by 4:

$$\begin{aligned}
 A &= \beta_3 \beta_2 \beta_1 \beta_0 \\
 (\beta_3)_{p3} &= (a_{n-1} \dots a_{\frac{3n}{4}})_r \\
 (\beta_2)_{p2} &= (a_{\frac{3n}{4}-1} \dots a_{\frac{n}{2}})_r \\
 (\beta_1)_{p1} &= (a_{\frac{n}{2}-1} \dots a_{\frac{n}{4}})_r \\
 (\beta_0)_{p0} &= (a_{\frac{n}{4}-1} \dots a_0)_r
 \end{aligned}
 \left. \vphantom{\begin{aligned} A &= \beta_3 \beta_2 \beta_1 \beta_0 \\ (\beta_3)_{p3} &= (a_{n-1} \dots a_{\frac{3n}{4}})_r \\ (\beta_2)_{p2} &= (a_{\frac{3n}{4}-1} \dots a_{\frac{n}{2}})_r \\ (\beta_1)_{p1} &= (a_{\frac{n}{2}-1} \dots a_{\frac{n}{4}})_r \\ (\beta_0)_{p0} &= (a_{\frac{n}{4}-1} \dots a_0)_r \end{aligned}} \right\} \begin{aligned} p_3 &= p_2 = p_1 = p_0 = r^{(n/4)} \end{aligned} \quad (3)$$

If the division's residue is 1:

$$\begin{aligned}
 A &= \beta_3 \beta_2 \beta_1 \beta_0 \\
 (\beta_3)_{p3} &= (a_{n-1} \dots a_{\frac{3n+1}{4}})_r \\
 (\beta_2)_{p2} &= (a_{\frac{3n+1}{4}-1} \dots a_{\frac{n+1}{2}})_r \\
 (\beta_1)_{p1} &= (a_{\frac{n+1}{2}-1} \dots a_{\frac{n+3}{4}})_r \\
 (\beta_0)_{p0} &= (a_{\frac{n+3}{4}-1} \dots a_0)_r
 \end{aligned}
 \left. \vphantom{\begin{aligned} A &= \beta_3 \beta_2 \beta_1 \beta_0 \\ (\beta_3)_{p3} &= (a_{n-1} \dots a_{\frac{3n+1}{4}})_r \\ (\beta_2)_{p2} &= (a_{\frac{3n+1}{4}-1} \dots a_{\frac{n+1}{2}})_r \\ (\beta_1)_{p1} &= (a_{\frac{n+1}{2}-1} \dots a_{\frac{n+3}{4}})_r \\ (\beta_0)_{p0} &= (a_{\frac{n+3}{4}-1} \dots a_0)_r \end{aligned}} \right\} \begin{aligned} p_3 &= p_2 = p_1 = r^{(n-1)/4} \\ p_0 &= r^{(n+3)/4} \end{aligned} \quad (4)$$

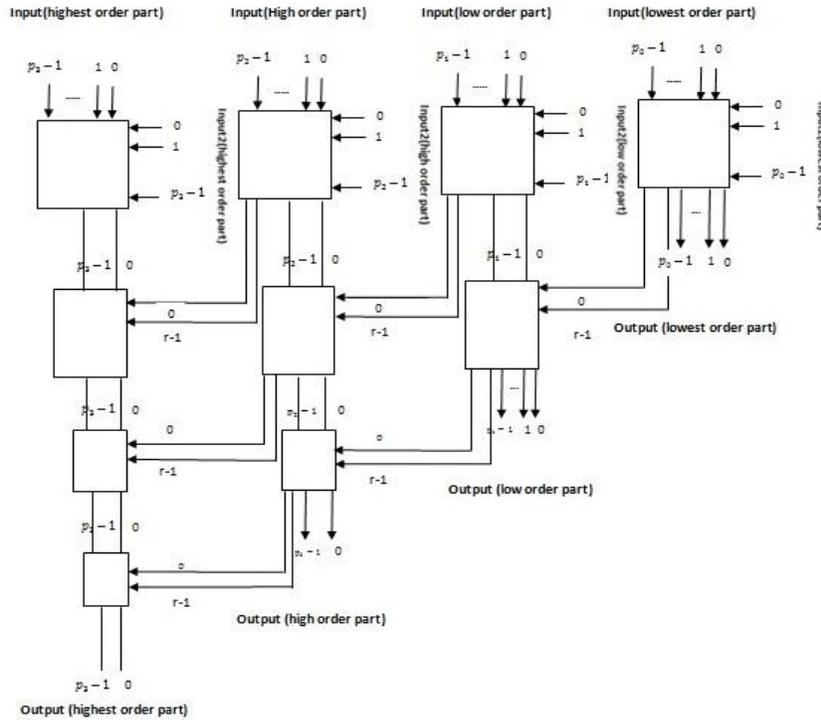
If the division's residue is 2:

$$\begin{aligned}
 A &= \beta_3 \beta_2 \beta_1 \beta_0 \\
 (\beta_3)_{p3} &= (a_{n-1} \dots a_{\frac{3n+3}{4}})_r \\
 (\beta_2)_{p2} &= (a_{\frac{3n+3}{4}-1} \dots a_{\frac{n+1}{2}})_r \\
 (\beta_1)_{p1} &= (a_{\frac{n+1}{2}-1} \dots a_{\frac{n+1}{4}})_r \\
 (\beta_0)_{p0} &= (a_{\frac{n+1}{4}-1} \dots a_0)_r
 \end{aligned}
 \left. \vphantom{\begin{aligned} A &= \beta_3 \beta_2 \beta_1 \beta_0 \\ (\beta_3)_{p3} &= (a_{n-1} \dots a_{\frac{3n+3}{4}})_r \\ (\beta_2)_{p2} &= (a_{\frac{3n+3}{4}-1} \dots a_{\frac{n+1}{2}})_r \\ (\beta_1)_{p1} &= (a_{\frac{n+1}{2}-1} \dots a_{\frac{n+1}{4}})_r \\ (\beta_0)_{p0} &= (a_{\frac{n+1}{4}-1} \dots a_0)_r \end{aligned}} \right\} \begin{aligned} p_2 &= p_1 = p_0 = r^{(n+1)/4} \\ p_3 &= r^{(n-3)/4} \end{aligned} \quad (5)$$

If the division's residue is 3:

$$\begin{aligned}
 A &= \beta_3 \beta_2 \beta_1 \beta_0 \\
 (\beta_3)_{p3} &= (a_{n-1} \dots a_{\frac{3n+2}{4}})_r \\
 (\beta_2)_{p2} &= (a_{\frac{3n+2}{4}-1} \dots a_{\frac{n+2}{2}})_r \\
 (\beta_1)_{p1} &= (a_{\frac{n+2}{2}-1} \dots a_{\frac{n+2}{4}})_r \\
 (\beta_0)_{p0} &= (a_{\frac{n+2}{4}-1} \dots a_0)_r
 \end{aligned}
 \left. \vphantom{\begin{aligned} A &= \beta_3 \beta_2 \beta_1 \beta_0 \\ (\beta_3)_{p3} &= (a_{n-1} \dots a_{\frac{3n+2}{4}})_r \\ (\beta_2)_{p2} &= (a_{\frac{3n+2}{4}-1} \dots a_{\frac{n+2}{2}})_r \\ (\beta_1)_{p1} &= (a_{\frac{n+2}{2}-1} \dots a_{\frac{n+2}{4}})_r \\ (\beta_0)_{p0} &= (a_{\frac{n+2}{4}-1} \dots a_0)_r \end{aligned}} \right\} \begin{aligned} p_3 &= p_2 = r^{(n-2)/4} \\ p_1 &= p_0 = r^{(n+2)/4} \end{aligned} \quad (6)$$

**Research Article**



**Figure 3: Symbol of novel adder**

Accordingly,  $\beta$  is in radix  $P$  and  $0 \leq \beta_i \leq p_i$  that  $\beta_3$  is the most and  $\beta_0$  is the least significant bit. For add operation in OHRNS same significant digits will be added. If we name those 4 parts as the least ( $\beta_0$ ), less ( $\beta_1$ ), more ( $\beta_2$ ) and the most ( $\beta_3$ ) significant, we can explain the adding method in this way, we add up least, less, more and the most parts independently based on One-Hot RNS, but we need the carry propagated from the lower part to the result of the addition of the higher part.(note that the carry in an adder in base  $r$  could be  $\{0, 1, \dots, r-1\}$ ). Figure4 depicts these algorithms precisely.

**Comparison**

We compare the conventional OHRNS to the proposed OHRNS in terms of propagation delay and the number of transistors and area.

-delay: 4 transistors. That means the circuit level enhancement causes the delay of this novel adder that is 4 times more than the conventional circuit.

-Area: The number of transistors used in conventional One-Hot adder is  $(r^n)^2 = r^{2n}$ . We can explain about the number of transistors in this new adder as below:

- If  $N$  is divisible by 4:  $4 \times (r^{n/4})^2 + 6 \times (r^{n/4}) \times r = 4 \times r^{n/2} + 6 \times (r^{n/4+1})$  (8)

- If the division's residue is 1:  $3 \times (r^{(n-1)/4})^2 + (r^{(n+3)/4})^2 + 6 \times (r^{(n-1)/4}) \times r$  (9)

- If the division's residue is 2:  $2 \times (r^{(n-2)/4})^2 + 2 \times (r^{(n+2)/4})^2 + 5 \times (r^{(n-2)/4}) \times r + (r^{(n+2)/4}) \times r$  (10)

- If the division's residue is 3:  $3 \times (r^{(n+1)/4})^2 + 3 \times (r^{(n-3)/4}) \times r + 3 \times (r^{(n+1)/4}) \times r + (r^{(n-3)/4})^2$  (11)

The area in this novel method is much less than the conventional OHRNS. For example for  $r=3$  and  $n=8$ , used hardware in OHRNS is equal to  $3^{16}$ , but in this method it would be  $2 \times 3^5$ . The proposed circuit is

### Research Article

divided to smaller parts and the number of used transistor layers decreased effectively, consequently the area drops down.

### CONCLUSION

RNS is used widely for high speed arithmetic circuits according to its carry free property and its smaller number nature which results in parallel arithmetic operation. OHRNS is a method which reduces the delay of addition and multiplication operation circuits to the delay of just one transistor.

This system is used in some applications require fast computation such as digital signal processing, digital filtering, image processing, RSA cryptography and generally for applications repeat addition, subtraction or multiplication operations in limited range of numbers .

In this paper a novel method for One-Hot adder is proposed which has significant improvement in term of applied transistors which is proportional to square root of the number of transistors, but increases the delay of operations.

### REFERENCES

- Abdallah M and Skavantzios A ( 2005).** On Multi Moduli Residue Number Systems With Moduli of Forms  $(r_a, r_b (1, r_c !1) )$  , *IEEE Transactions of Circuits System* **52**(7).
- Farshidi R, Zadnavin AH and Gholami E (2010).** A novel multiple valued logic OHRNS adder circuit for modulo  $(r^n-1)$ . *The 4th International Conference on Advanced Engineering Computing and Applications in Sciences, ADVCOMP* 166-170.
- Hosseinzadeh M, Jassbi SJ and Navi K (2007).** A novel multiple valued logic OHRNS modulo  $r^n$  adder circuit. *Proceedings of World Academy of Science, Engineering and Technology* **25** 128-132.
- Labafniya M and Eshghi (2010).** An efficient adder/subtractor circuit for one-hot residue number system. *International Conference on Electronic Devices Systems and Applications (ICEDSA)* 121-124, 11-14.
- Ramirez J et al., (2002).** *Fast RNS FPL-Based Communications Receiver Design and Implementation, Proceedings of 12th International Conference on Field Programmable Logic* 472- 481.
- Somayeh Timarchi and Keivan Navi ( 2009).** Arithmetic Circuits of Redundant SUT-RNS, *IEEE Transactions on Instrumentation and Measuremen* **58**(9).
- Taleshmekaeil DK and Mousavi A (2010).** The use of residue number system for improving the digital image processing. *IEEE 10th International Conference on Signal Processing (ICSP)* 775- 780, 24-28.